

# THE pcb DESIGN MAGAZINE

August 2017

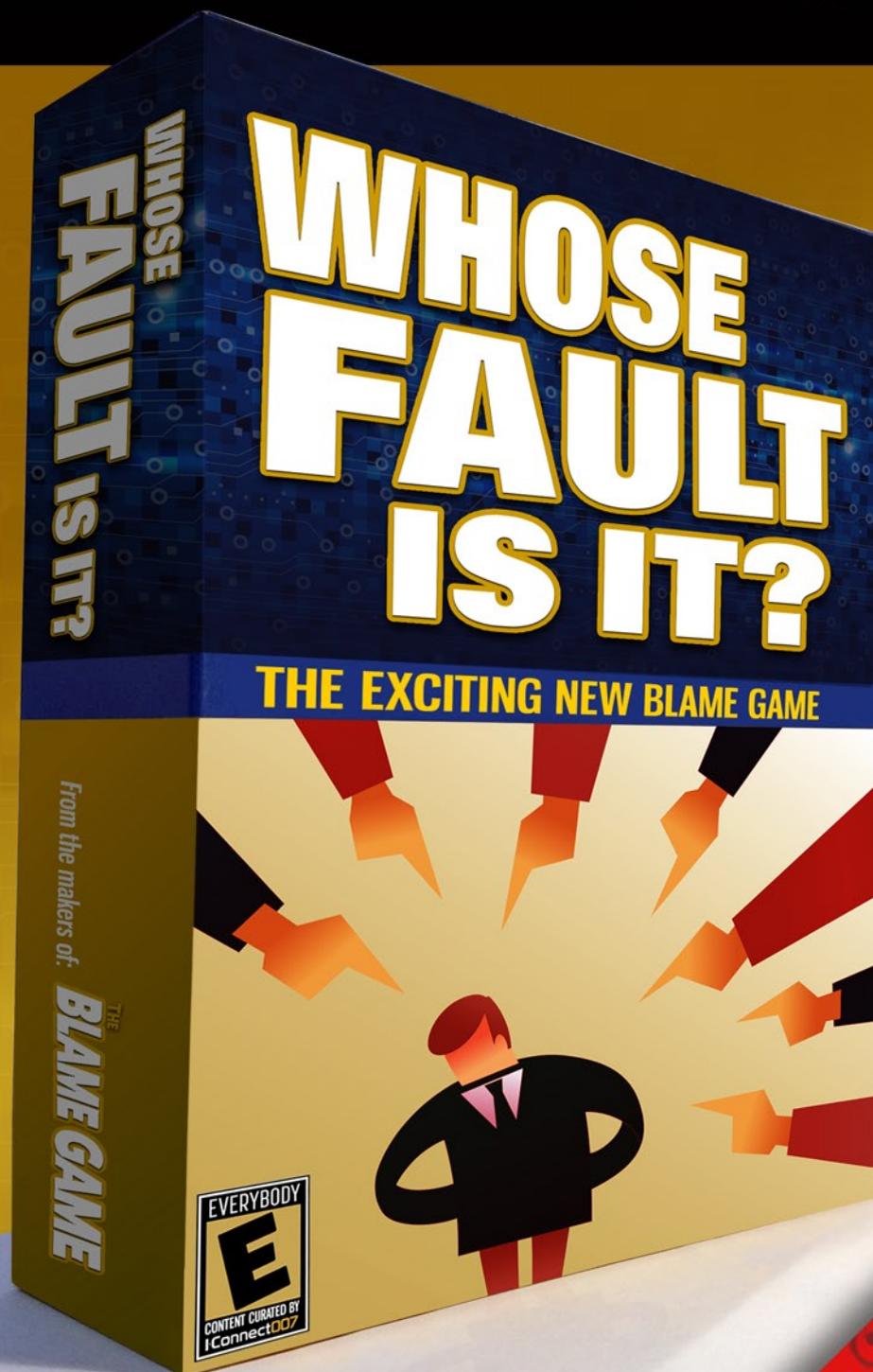
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## Whose Fault is It?

What does your company do when a board fails? When the board is designed, fabricated and assembled by three different entities, not to mention shipped by a fourth, figuring out what went wrong can be difficult, not to mention time-consuming.

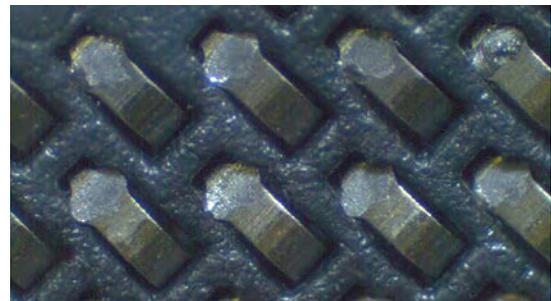
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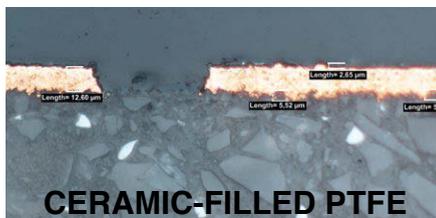
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# Engineering And Providing Balanced Interconnect Solutions



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# Mist<sup>e</sup>aks Were Made

by Andy Shaughnessy

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Let's just state for the record that no one wants to make a mistake.

I think it's just a matter of human nature. It starts in elementary school; nobody wants to stand in front of the class at the blackboard and get a math problem wrong. If you do, it's a long walk back to your desk!

Yes, we humans hate to face the looks of opprobrium from our fellow man. So, we go out of our way to avoid making mistakes.

The PCB industry is no different. Fortunately, PCB designers, design engineers, fabricators, and assembly providers generally do what it takes to create a PCB that functions in the field as desired. But mistakes do happen.

What does your company do when a board fails? When the board is designed, fabricated and assembled by three different entities, not to mention shipped by a fourth, figuring out what went wrong can be difficult, not to mention time-consuming.

Naturally, we're approaching this equation from the point of view of the PCB designers and design engineers, because they tend to bear the brunt of the blame when a PCB starts smoking.

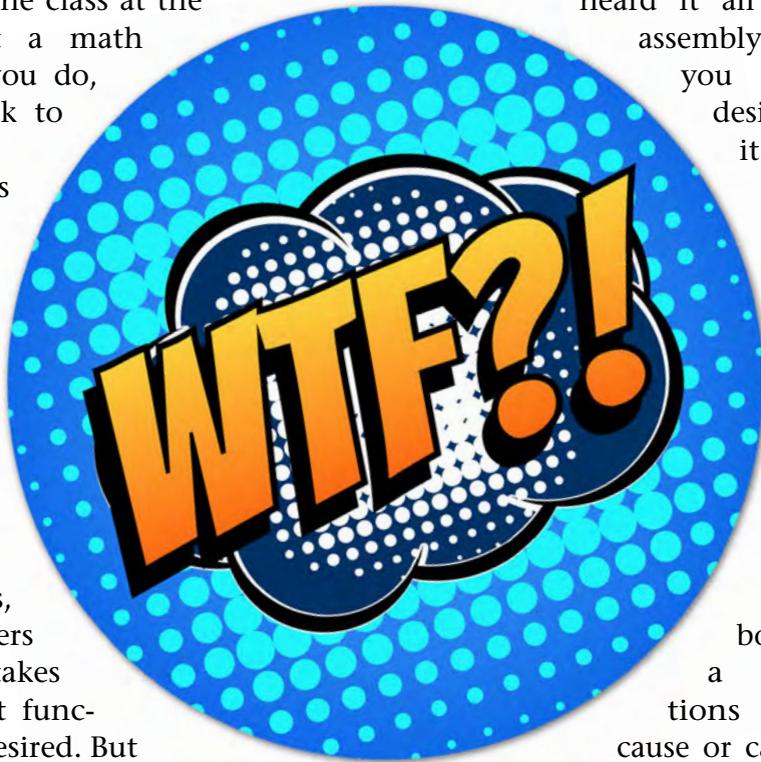
And design is at the front end, so PCB fabricators and assemblers have no problem casting a suspicious eye upstream.

I'm sure you designers have heard it all from the fab and assembly folks: "How did you all screw up that design so badly? We built it the way you wanted it. Don't your software tools do most of the real work for you? Turn off the Pink Floyd and get cracking!"

We started planning this issue with a survey sarcastically titled, "Whose fault is that bad board?" We asked a variety of questions regarding how the cause or causes of failure were determined, and what companies do to keep from making the same mistake again.

We asked the question "If a board fails in the field, whose fault is it, typically?" Here are some of the answers, slightly edited for clarity:

- Equipment set-up not followed, test procedure not followed, and demo manual not adhered to.





- The component manufacturer's.
- We put our boards through a lot of testing before they get to the field. It is usually an unforeseen stress or other phenomenon that instigates the failure.
  - This is twofold: The last person to handle the assembly and the final failure analysis outcome results.
  - As far as the designer's responsibility, in most cases difficult technologies are discovered before the order is accepted, if not shortly thereafter. This affords an opportunity to improve upon the original design in concert with the designer, resulting in a potential savings in time to manufacture and cost to the customer.
  - It could be anyone's fault. It can be the designer plus the fabricator, the fabricator plus assembly, or it could even be everyone's fault.
  - The designer. By designer, I mean the board architect (the guy who chooses the devices), the design engineer who does the schematics, a lack of SI/PI engineer, and the CAD engineer (who is doing a high-speed board without adequate and relevant knowledge).

We asked, "If you, the designer, are truly at fault, how do you avoid making the same mistake again?" Answers included:

- Keep a log of past and present faults, ensure your checkers and design rules are properly set-up, and always check your work. It doesn't hurt to have a peer review.
- We put in place and modify processes to cover the cause and verify that we don't do it again. We call it DIVE: Define the issue, investigate why, verify the fix/correction, and ensure it's corrected by monitoring designs that follow.
  - By changing the company design procedures and sharing the information with my colleagues and network.
  - We designers expect our manufacturing counterparts to be able to inspect and verify, qualify and certify every phase of the PCB manufacturing process so that if a problem arises, we can issue a corrective action report. We expect the supplier to be able to comb through their

processes to find out where and how a defect occurred and document how they are going to fix the process so that it won't re-occur. Aren't we designers playing the hypocrite if a layout problem is found and we cannot point to a design process?

As you can see, there are no easy answers. Everyone plays a part in the board's development, and everyone is a suspect. So, this month we asked our expert contributors to discuss methods for identifying the cause of board failure, and steps to take to avoid repeating this mistake in the future. (There's also a little bit of finger-pointing, of course.)

First, Gaudentiu Varzaru of the Politehnica University of Bucharest discusses all the ways for problems to creep into a PCB design, including overly automated EDA tools. Scott Decker of UTC Aerospace Systems explains why no one has the right to point fingers—there is plenty of blame to go around when a board fails. EPTAC's Kelly Dack focuses on the use of root cause analysis, and how RCA can help technologists quickly find the cause of failure and make sure it never happens again. And consultant Tim Haag explains how tough it is to find the root cause. He shares a few horror stories about failures that were not his fault, despite what everyone else thought at first.

And we have columns from our regular contributors Barry Olney and John Coonrod. We are also introducing Jade Bridges of Electrolube, whose first column focuses on coatings for thermal management.

It's almost the end of summer, and trade show season is around the corner. We'll be at PCB West and SMTA International in September. I hope to see some of you on the road! **PCBDESIGN**



**Andy Shaughnessy** is managing editor of *The PCB Design Magazine*. He has been covering PCB design for 18 years. He can be reached by clicking [here](#).

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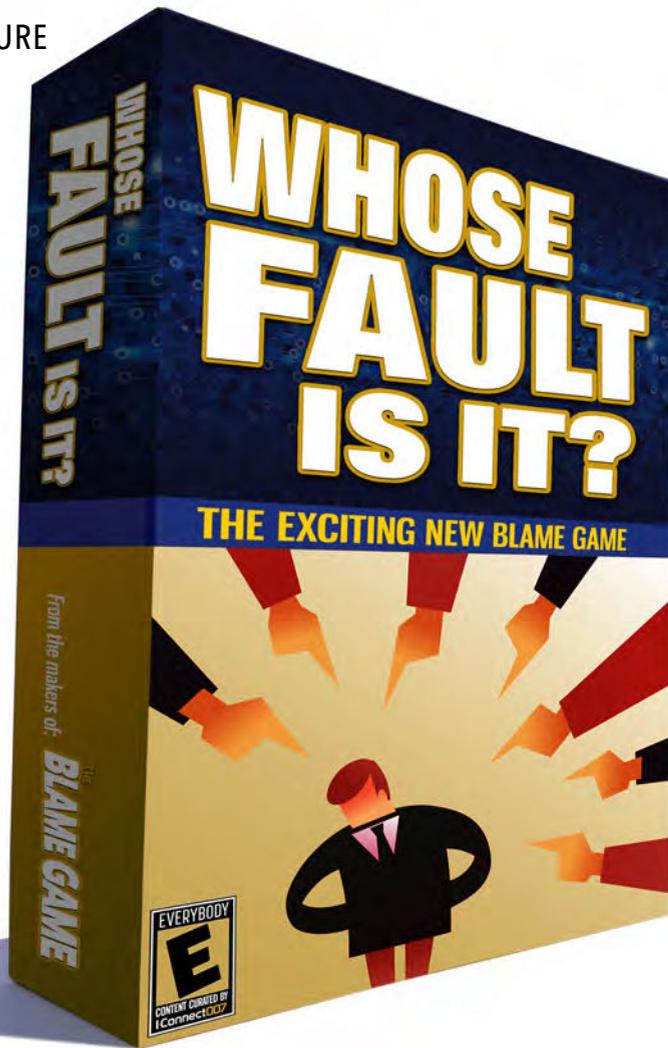
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# Whose Fault is That Bad Board?

## Gaudentiu Varzaru

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Not long ago, I answered Editor Andy Shaughnessy's "Whose Fault is That Bad Board?" survey. When I answered the first question ("If a board fails in the field, whose fault is it, typically?"), I was disappointed that he used radio buttons instead of check boxes. I did not want to blame only the designer for every bad board in the world. Did Andy want me to name the ones who are most often blamed?

Who are these designers? PCB designers are like magicians; they can materialize an idea from a piece of paper, and many of them are also the creators of the product. And designers create many jobs. Their projects may have gaps, but I would not blame designers for all the bad boards. They are the first to be blamed because they take the first step in the product's life cycle. They can make mistakes too, but sometimes their fault is having too much confidence in the people who follow up on their work.

I know an American entrepreneur who went to Poland to open a PCB design bureau. He found painters and architects for hire, but not many engineers; he was very pleased to find many electronic engineers here in Romania. But are all engineers qualified to be great PCB designers?

Year ago, I held a position in an EMS company where projects were analysed before sending them to be produced on the assembly lines. We found that even some of the best and most innovative circuits could not be manufactured. Why? Because the PCB designer, an electronic engineer, was not acquainted with the fabrication process. He had no idea about technological requirements necessary for electronic production.

Here is a funny story: I know of one designer who learned, finally, the importance of the thermal relief pad for heat restriction during reflow for a good soldering. His response? "Oh, was that what they were for? And to think I worked so much to remove them!"

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The CAD program itself had introduced thermal bridges where the pads were linked to large copper areas, but the designer's eye did not like the way they looked. This was a happy case because the designer had presented the project before sending the order for fabrication. But other times, matters were much more serious. When a board came in for assembly, it was necessary to manually heat the pad and the component with two soldering irons. Some designers understood this aspect (especially after they were walked through the factory to see the whole technological process), while others even got angry, yelling, "I will send the project to China and they will do it!" Yes, they will, but they will fabricate exactly what was sent, including the design errors. This was the case once when a designer forgot to send an Excellon file; the printed circuit board was manufactured without the holes for the 40-pin DIL package of a microcontroller.

Some designers will gladly fit the schematic on the entire sheet. One designer learned that, with the right modifications, the area of the printed circuit board could be reduced, and thus the cost of the board could be reduced. He replied, "Oh, it is for the Army, and they have enough money not to worry for the size of the board!"

I think such an army has lost the battle even from the design stage: More materials mean heavier weapons, more fuel consumption for transportation, larger pack sizes, less weapons, less money for further development, and so on. So, in order to be a professional designer of today's electronics, it is not enough to be an electronic engineer; it is also necessary to have the proper technological knowledge, or to team up with a technologist. This is one reason that we decided to include a DFM course in the electronics curriculum at my college.

Nowadays, printed circuit boards are more complex. Many PCBs now have controlled impedance requirements. Flex-rigid is more popular than ever, and we're seeing glass circuit boards and many metal-backed PCBs. They have become dedicated passive components; some are even active, such as the embedding technology from Würth Elektronik, which can embed flip-chips within the multilayer struc-

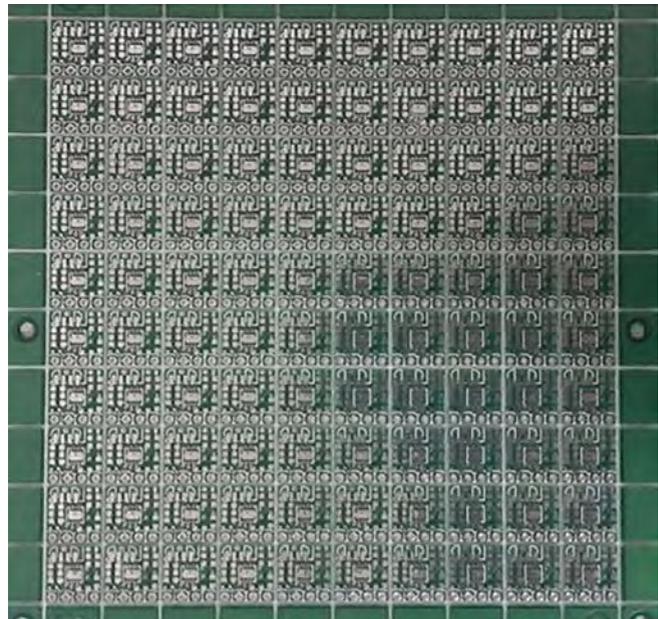


Figure 1: V-cut panelized 10" x 10" circuit board.

ture. Moreover, an assembled electronic module may have several thousand solder joints, which are also components.

As my colleague Ioan Plotog used to say, "Solder joints are living things." They are not immutable; due to the environmental conditions, different kind of stress (mechanical, thermal) and aging, they are changing outside (tin whiskers), and they are changing inside (microstructure), so their electrical, mechanical and thermal functionalities are affected. It is known that ESD issues may hit a long time after the product is launched into the market.

With circuit boards, one hand doesn't always know what the other hand is doing. For example, did the component supplier or the electronic assembly provider respect all the preventive procedures against electrostatic discharge? I heard about a board that functioned on a rack, but stopped functioning when it was removed and inserted into another rack several meters away. That was the day when the operators from the electro-mechanical telephone exchange discovered that walking on carpet charges you with several thousand volts and the circuit layers of the electronic module must not to be touched. The cleaning of the boards is another problem which may have a delayed effect due to electrochemical migration.

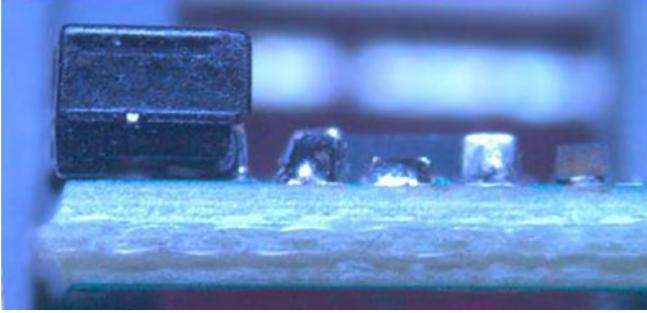


Figure 2: The component could have been damaged if a PCB depaneling machine were used.

Once, a customer brought in a panel board for assembly. The panel contained 100 pieces arranged in 10" x 10" small circuits for V-cut (Figure 1). In order to print the solder paste onto the board, a stencil had to be manufactured. The designer didn't have the Gerber files for the panel, but for a single circuit. However, when the design of the panel was ready, it was observed that the dimensions of the panelized project did not fit the dimensions of the physical panel. We searched for the cause, and we concluded that the PCB manufacturer did not make the V-cut panelization according to IPC standard recommendations; instead, the board shop took the V-cut spacing from the useful area of each circuit. This led to a manual depanelization in order to avoid component cutting by the depaneling machine.

This is an example that can be classified as a fault on the side of the PCB manufacturer because their operators did not follow the IPC-7351A "Generic Requirements for Surface Mount Design and Land Pattern Standard" recommendations. Therefore, we have decided that our faculty should include IPC standards (especially 2221, 2222, 600, 610, 7351) in the curriculum package for our engineering students. However, as I used to say to the young student designers, "Do not let others decide for you. Send complete information!"

Here is an example of a chain of mistakes featuring three actors. The electronic module was not working properly at the final test made on the customer's premises. After investigating the situation, it was found that certain PCBs presented defects like interrupts and badly plated vias. The boards did not present any trace of

test needles, so it was concluded that the manufacturer of the printed circuit board did not perform the electric test, and some boards passed through, although they were defective. Later, the manufacturer agreed that their secondary facility in China did not do the job properly. Here is the first mistake: The PCB manufacturer did not follow test procedures. The electronic assembly manufacturer did not check the bare boards at the incoming quality department because he had too much confidence in the quality of the Korean PCB company's products. That was the second mistake: The electronic assembly manufacturer did not follow test procedures again. He assembled all the boards and after a routine optical inspection, and he concluded that all the components were correctly soldered. The PCB designer did not supply the test procedure for the assembled electronic module, so the EMS company delivered the boards without testing them, except for the optical inspection of the solder joints. This was the third mistake: the customer did not deliver to the EMS company any test method for the assembled boards. The bad boards could not be repaired satisfactorily, so all the electronic components (a total cost of over US\$1,200) were lost.

Yet another chain mistake example: When trying to fix the BGA capsule in a socket, it detached very easily from the PCB (Figure 3). Of the 12 sockets on the same electronic module,

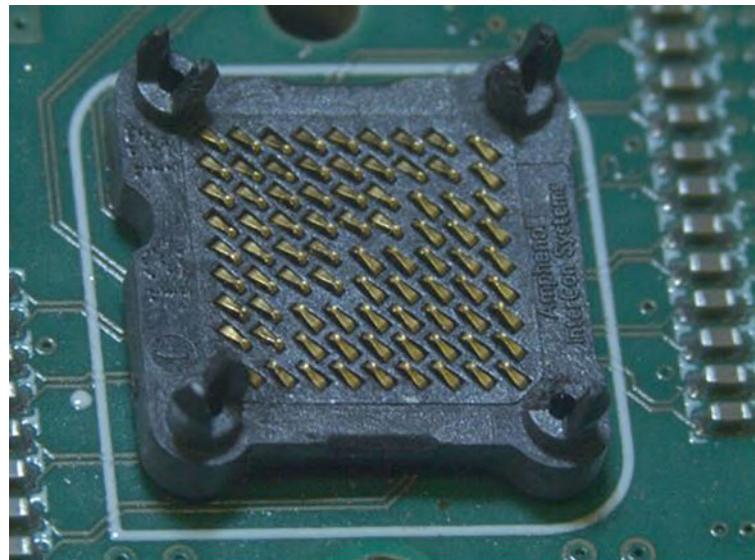


Figure 3: The BGA socket.

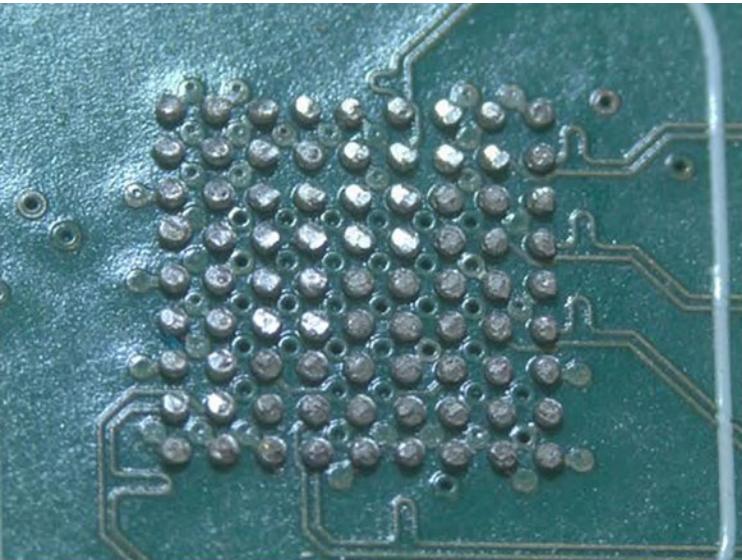


Figure 4: The solder paste melted and formed the joint with the balls of the socket.

four had this problem. Going back on the route traveled by the electronic module, the following mistakes and miscues were found: A customer (also a designer) ordered the manufacture of a very expensive board to an EMS company, providing all the components except for one—a 1,156-ball FPGA, which the distributor could not deliver together with the whole bill of materials (BOM). This was the first mistake: Assembling a board without a complete BOM.

Having in mind that a third reflow process would be necessary for FPGA assembly, the technicians from the EMS company assembled one side of the board with lead-free solder paste, and the other with tin-lead. They assumed that during the second reflow process, the solder joints from the first side would not melt and the component would not drop in the oven. This was the second mistake: They mixed the solder alloys SAC with SnPb; the FPGA contained SAC alloy balls. In order to solder the new FPGA onto an 18-layer FR-4 board with components on both sides, a lead-free soldering thermal profile was used. The thermal process took place on an SMT rework and repair station using hot air for upside heating and infrared radiation for backside heating.

Inherently, the heat affected the components in the vicinity of the FPGA package, sev-



Figure 5. Where are the balls?



Figure 6: Is this new component good or fake?

eral BGA sockets among them. According to the datasheet, these sockets had SAC balls, but they were previously soldered with an SnPb alloy, too. At first glance, the solder paste melted and made joints with the socket balls (Figure 4). However, it was very curious to see that almost not a single ball remained on the socket's spring (Figure 5). It looks as if, instead, the ball was not properly attached to the socket's spring. Could it be a fake component (Figure 6)? This problem of distribution is another cause of bad boards, which seems to never stop.

When a chain mistake occurs, the rule of 10 comes into play. The Latin expression "quod erat demonstrandum" is illustrative.

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You may think that none of this provides an answer to Andy's simple question, because in none of these cases did the board reach the client; this all happened inside the production stage. Who was at fault when a defect of the airbag system forced Nissan to withdraw cars from the market due to a bug in the cruise control deactivation switch manufactured by Texas Instruments? The PCB designer? The electronic module manufacturer? The car manufacturer? Everyone?

Why, despite the many DfX initiatives (including Design for Zero Defects and Design for Six Sigma), do these errors still happen? Basically, rules are for humans.

I read an opinion column recently that described robotization as the single best way for America to bring back electronics production from China. If this happens, will the mistakes disappear?

No, not if the robots are controlled by humans. As another old Latin saying goes, "Errare humanum est." **PCBDESIGN**



**Gaudentiu Varzaru** is a researcher at the Politehnica University of Bucharest and a show manager for the TIE PCB design conference.

## LMU Finds New Way to Tune LED Colors

The color of the light emitted by an LED can be tuned by altering the size of their semiconductor crystals. LMU researchers have now found a clever and economical way of doing just that, which lends itself to industrial-scale production.

Unlike the incandescent light bulb, LEDs produce light of a defined color within the spectral range from the infrared to the ultraviolet. The exact wavelength of the emission is determined by the chemical composition of the semiconductor employed, which is the crucial component of these devices. In the case of some semi-conducting materials, the color can also be tuned by appropriately modifying the size of the crystals of which the light-emitting layer is composed. In crystals with dimensions on the order of a few

nanometers, quantum mechanical effects begin to make themselves felt.

LMU researchers in collaboration with colleagues at the University of Linz (Austria) have now developed a method for the production of semi-conducting nanocrystals of defined size based on the cheap mineral oxide known as perovskite. These crystals are extremely stable, which ensures that the LEDs exhibit high color fidelity—an important criterion of quality. Moreover, the resulting semiconductors can be printed on suitable surfaces, and are thus predestined for the manufacture of LEDs for use in displays.

The crucial element in the new method is a thin wafer, only a few nanometers thick, which is patterned like a waffle. The depressions serve as tiny reaction vessels, whose shape and volume

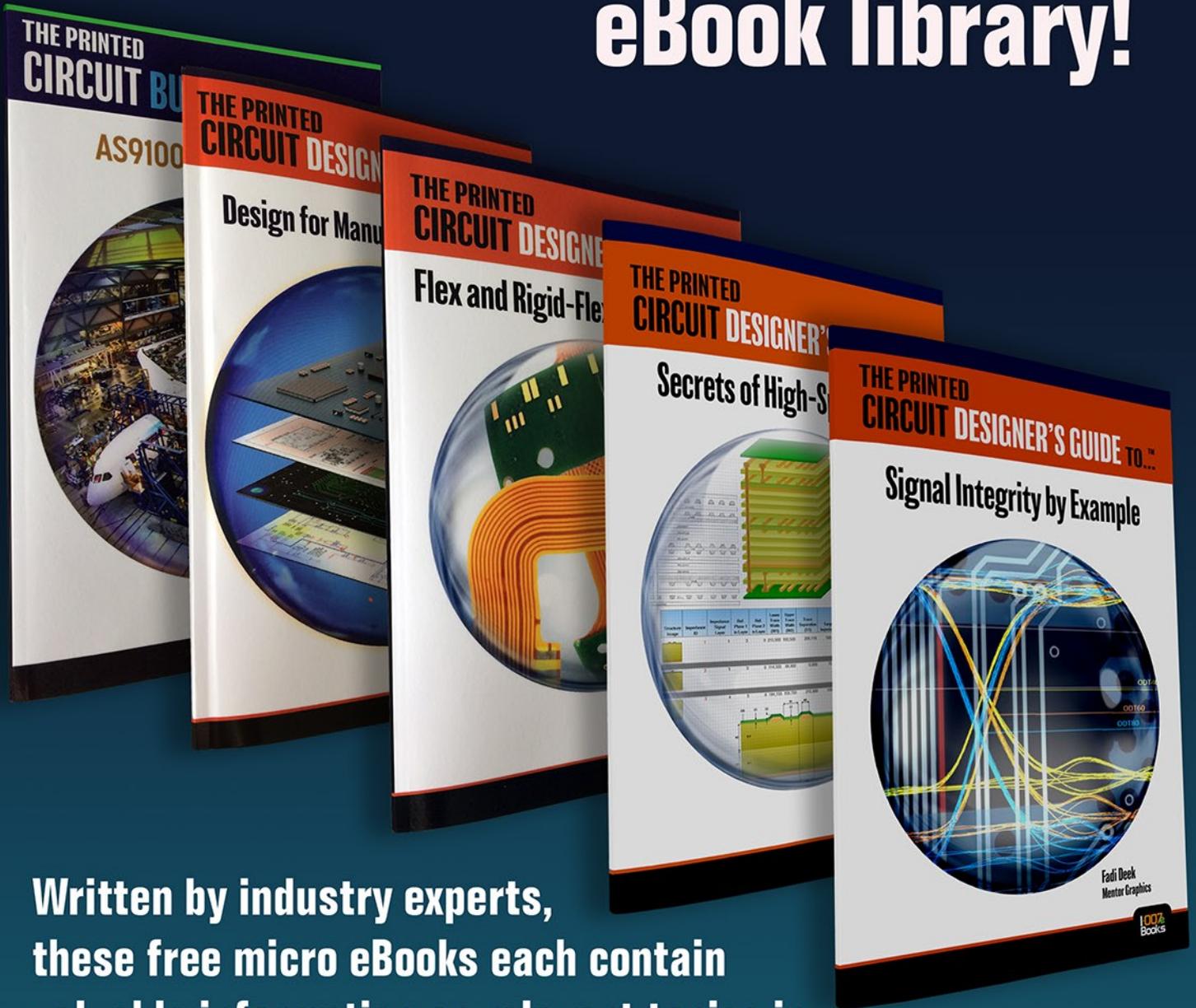


ultimately determine the final size of the nanocrystals. "Optimal measurements of the size of the crystals were obtained using a fine beam of high-energy X-radiation at the Deutsche Elektronen-Synchrotron (DESY) in Hamburg," says LMU researcher Dr. Bert Nickel, member of the Nanosystems Initiative Munich (NIM), a Cluster of Excellence.

Moreover, the wafers are produced by means of an economical electrochemical process, and can be fashioned directly into LEDs.



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# Enough Blame to Go Around

by **Scott Decker, CID+**  
UTC AEROSPACE SYSTEMS

The idea for this article began a few months ago when *The PCB Design Magazine* conducted a reader survey regarding the topic “Whose Fault is that Bad Board?” After some thought, I submitted my answers. After all, I must have some kind of input after over 25 years of PCB design. But still, whose fault is that bad board?

Most of a PCB designer’s job involves placing parts and routing traces on a CAD tool, and then whipping out a set of drawings and Gerber files to send to the fab shop. Some of you even draw the schematics and maybe even do some library work now and then. For me, I’ve done all of that and more over the course of my career. That doesn’t make me a great designer; it just says I’ve done a lot of different things, as I’m sure many of you have too. So when it comes to problems with PCBs, just who is really at fault, and what do you do about it when you have issues, big or small?

As designers, we are typically detail-oriented and most likely perfectionists when it comes to



our design work. I’ll admit it: I could clean up routing for days, but I limit myself to an hour or so per layer, as hard as that is for me sometimes. Unless it’s in-our-face obvious, when we try to decipher what happened when we have issues with a board, we tend to look someplace else.

OK, I know what you’re thinking: Don’t go there. We designers make mistakes too. Some of the things I’ve learned along the way came from making mistakes, and as we all know, that’s how you learn. As an example, and I have lots to choose from, once in my early days of design, the drawing checker asked if I could remove the leading zeros from dimensions under one inch. I thought about it. I really didn’t want to do this, because the zeroes are interactive with things on the board. His reply was that if I could possibly do so, then take the leading zeroes off any dimensions under one inch.

Against my better judgement, I did it anyway, and not more than a couple of weeks later, I get a call from the fab shop. It seems they started routing into one of the boards in a six-up panel. After I did a little investigating, I remembered that I changed the frame outline a



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bit and, you guessed it, the dimension didn't update. Once I got the panel from the shop, I proudly took it up to the checker and exclaimed, "See, this is what happens when you override a dimension!" His answer was, "I just said to remove them if you could, not that you had to." So, whose fault was that? His for requesting that I remove them, mine for doing it when I knew I shouldn't, or me for not remembering I did it or maybe not providing a compelling reason not to? After that, I had a good reason for leaving the leading zeroes alone, no matter what the dimensions are. Lesson learned.

.....

“Hey, if I designed it, I should have a good idea what the PCB should look like when it hits the door, right?”

.....

Many years later and just as many lessons, I found myself doing design, libraries, schematic work and now serving as an incoming inspector for all bare PCBs. Hey, if I designed it, I should have a good idea what the PCB should look like when it hits the door, right? So, I get some boards in that have little perfectly curved crescent "mouse bite" shapes in the pads and traces all over the board. This is where IPC's Tech Net really shines and I recommend everyone to sign up for it. I had never seen anything like that before, so I posted a question to the forum. About a day later, I got a reply. It seems that bubbles in the etching tank can stick to the copper if not rinsed or knocked off by agitators in the tanks. After a couple of exchanges of related questions, I get a call from the QA manager of the company that did our boards. Turns out he was the guy on Tech Net who told me about this issue, and when he put my questions to the problems he found in his own shop, a light went on in his head and he knew that this was the culprit. The boards were replaced and never should have left the shop. Designer 1, fab shop 0, but who's keeping score?

OK, so I've hit the designers and the fab shops, and now it's the engineers' turn in the barrel. Yes, despite what some will tell you, engineers don't know everything about PCB design. For example, I once had a simple requirement for a controlled impedance board that needed 65 ohms for a PCI bus and 50 ohms for everything else. Well, it's not always that easy when you are trying to keep a minimum 5/5 on the design and the board is packed with parts. Since the 65 ohms was only needed on the outer layers, the internals were easy to hit 50 ohms. Well sort of.

I went around and around with the fab shop working on a stackup that would give me those golden impedance numbers, but alas, I just couldn't get 50 ohms. About as close as I could get with this really densely packed board was about 56 ohms routed with an approximately .012" trace. On that board, it was like building a freeway through a residential area without moving a house. I checked with the engineer each time I got new numbers and he said that 58 ohms is fine. But he said he really wanted it as close to 50 ohms as I could get.

Yep, I ripped it up and re-routed it with 56 ohms. After the second set of numbers and ripping up both internal and external routing, I asked the engineer why he needed the 50 ohms so badly. After all, the board was mostly analog and the digital stuff wasn't fast, so what's driving the 50 ohms? As a former engineering technician, I really wanted to understand this design requirement. His answer was, "Well, I just wanted to be sure all of the layers were the same impedance."

At that point, I was standing there with a puzzled look on my face and really hoping I wouldn't get the answer I was going to get, but I asked anyway. "If all you want is for all the impedances to be the same, could they all be 65 ohms?" His answer could have got me thrown in jail had I picked up the chair close by, but he said, "Sure, as long as it's the same on all the layers. That's fine." I re-routed for the third and last time, the board was all 65 ohms on all layers and all 5/5 spaces and traces. Case closed. I'm not really sure how to score that one.

Now, after reading over these examples, it's easy to see that everyone can play a part in the

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“Blame Game.” We put into place all manner of processes, work instructions, checklists and the like, all in our quest to try to prevent bad things from happening to our boards, and for the most part, these processes work. But let’s face it; we are human and we make mistakes. We build checks and balances into our processes and do the best we can, but it happens. It can be at the engineering start, or the requirements for the device, or the design requirements, all the way to the assembly, so where do we really put the blame? In many of these cases, it’s as simple as just good communication. Communication can be the key to so many things, and these types of issues are no exception. I’m sure you’ve heard the saying that there is always enough blame to go around.

“Communication can be the key to so many things, and these types of issues are no exception.”

So, one last story to make your day, this time focusing on the value of good communication. Again, many years ago, a new local fab shop called me and practically begged me for work so they could show how good and fast they could be. I finally said sure.

I had this little board about 1.5” x 1.5” with all of three or four parts on it. What could go wrong? After the week of lead time went by, I got a call from the guy at the fab shop. He said the boards are all done (about 250 of them), and everything looks great except one thing. I thought, “Hmm. You do remember I’m that new customer that you really wanted to impress, right?”

Anyway, he says that all of the boards are about .025” too small. He goes on to explain that the guy that runs the milling machine was out sick, so he stepped up to do the job. This was a small company, as you may have already realized, and he noticed the spindle on

the machine was wobbling a bit and the bearings needed to be replaced. Once that was done, he proceeded to route the boards, but what he didn’t know was that his router operator knew that the bearings were bad and compensated for the wobbling. Seriously.

Since the boards were assembled using holes in them, the edges were not really critical, so I accepted them at a slight discount. Later that day I got a call from the front desk when he delivered them, and went up to chat with him about the issue. I was told he dropped them off and left. I’m not sure if he left rubber in the parking lot when he did, but he never called for more work, and I just couldn’t find it in my heart to call him for the next job.

So there you have it: There’s plenty of blame to go around. I didn’t even mention the \$250,000 board error, but maybe some other time. I’m sure many of you have horror stories that are even worse, and I didn’t even make a dent in my 25 years of design. When any of us have an issue—including designers—we need to look at each case individually and really ask if we could have done something to keep that from happening. You bet there will be cases where we can say, “Nope, this one is on the other guy.”

But remember that you may be the other guy sometimes too. If you are new to the design world, it will be a learning experience for you, just like mistakes have been. Additionally, listen to the designers who have been around for a while and learn what you can. The veteran designers can be a big help—trust me. If you have been around the routing outline a few times, you’ll know it happens to the best of us.

I’m not an expert in design, and I can prove it sometimes. But at the risk of dating myself, I leave you with the wisdom of Laugh In announcer Gary Owens: An “ex” is a has-been and a “spurt” is a drip under pressure. I have no desire to become an expert, but I would like to know a lot. Happy routing! **PCBDESIGN**



**Scott Decker, CID+**, is staff engineer in PCB design services at UTC Aerospace Systems’ Electronic Systems Center.



# 2017 Programs

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## July 26-27

### IPC Technical Education

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## September 16-21

### IPC Fall Committee Meetings

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## October 3-4

### IPC & WHMA Wire Harness Manufacturing Conference

Paris, France

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## October 3-4

### IPC Technical Education

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## October 9-10

### IMPACT Europe

Brussels, Belgium

Meeting

## October 17-18

### IPC Flexible Circuits-HDI Forum Conference

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## November 8

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## November 14-17

### IPC Committee Meetings

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Meeting

## November 14-17

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## December 6-8

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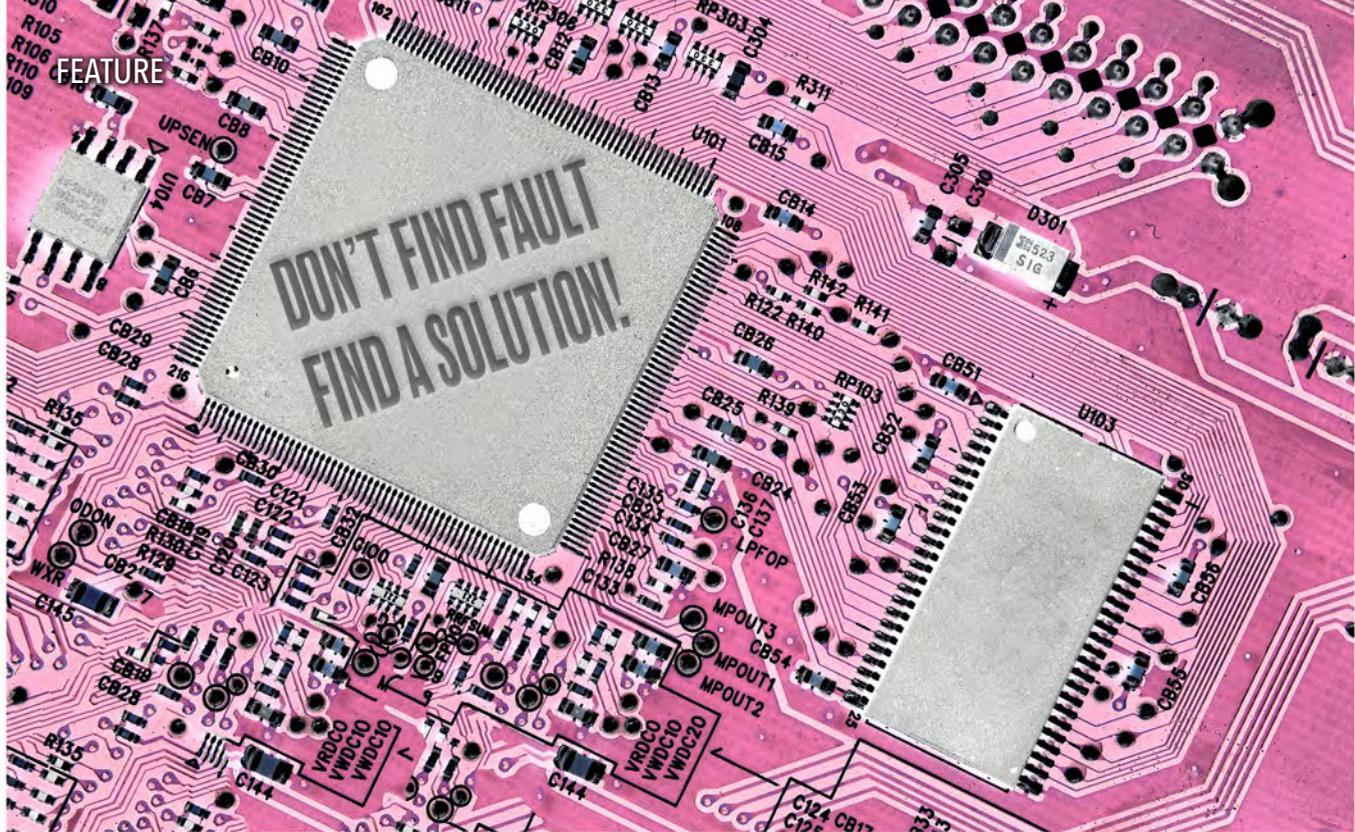
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## FAULT-FINDING: IT'S ALL ABOUT PREVENTION, NOT BLAME

by Kelly Dack, CID+  
EPTAC

There are thousands of things that can go wrong during the design and manufacture of a PCB assembly. One might say that it is an absolute miracle when a PCB goes through all of its phases—design, fabrication and assembly—and operates successfully!

But what happens when something goes wrong? The flow of an entire project can be disrupted when a problem is discovered on the PCB. What happens when a short or an open circuit is discovered; a part lead won't fit into a hole or an entire connector pattern is designed backward? Murphy's Law ensures us that PCB issues are discovered at the most critical periods of a PCB's design and manufacturing cycles.

So, it is not a question of if a problem might be found, but when. A designer must be aware that their management and their customers may be less in tune with the technical aspects of the why their design is running late or doesn't work. But like the Queen of Hearts in "Alice in Wonderland," there are some management and customer cultures out there who naively at-

tempt to resolve problems by seeking out the culprits and shouting "Off with their heads!"

Seasoned PCB designers have learned that jumping to a conclusion without carefully examining all of the possibilities is not only a waste of time, but can be devastating to the carefully cultivated relationships. A quick read of almost any psychology article on "fault" or "blame" will coax the reader away from adding to a problem by placing fault or blame on others. It is far more productive to examine yourself first before shining forth as part of a solution. Focus on process rather than personalities.

Companies in the PCB industry have adapted a widely accepted methodology for sleuthing out the source of problems which might occur during a product development cycle: root cause analysis<sup>[1]</sup>. Root cause analysis (RCA) began in the 1950s as a study by NASA and had its origins in rocket design. RCA methods are used to methodically identify root causes of events, rather than to simply address the symptomatic result.

Note that root cause analysis does not get personal and does not name names or specific function. RCA is not a witch hunt to determine

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who's at fault. It is more of a 10,000-foot flyover of a project or process, tailored to determining where, in a progression of events, the root cause of a problem occurred so that it can be identified and corrected.

Once an organized, logical, process-oriented approach has been implemented in order to determine the root cause of a problem, what is the next step? How can we best convey the results? We are fortunate that our PCB manufacturing industry stakeholders have been around long enough to establish successful processes and can usually recognize when a process needs to change or evolve. PCB manufacturers are very familiar with a form of communication between customer and supplier known as the corrective action report (CAR) request. When an unacceptable problem is identified by a customer, it is common for the customer to issue a CAR request to the supplier as a form of good business practice and clear communication. The CAR request is intended to communicate that a problem was found and determined to be rooted somewhere in a process owned by the supplier. The CAR request is carefully generated to identify and define the problem, such as a non-conformance issue relating to a hole size or finish defect and respectfully convey it to the supplier. Simply, the CAR protocol requests the supplier to perform three basic steps in order to improve their process so business can continue:

- 1) Acknowledge ownership of the defect.
- 2) Be able to point to an established process and identify where the defect occurred, when it occurred and how it occurred.
- 3) Be able to explain to the customer how the process shall be corrected so that the problem will not occur again.

Let's face it. Problems happen within any system with human involvement. Mistakes will be made, and process will break down. How the call-and-response format is tendered will affect the success of both parties. Hopefully your design team will see that a compelling CAR protocol between customer and supplier is far more propulsive to product success and good business than a desperate call for a merciful beheading.

RCA stresses that preventing a future snafu

is far more important than identifying the actors responsible for the current foul-up. When a customer issues a CAR request, a general process for performing and documenting RCA corrective action on the part of the supplier is outlined like this:

### **That Day we Received Pink PCB Assemblies**

Oh, if our engineering, manufacturing and purchasing groups had only possessed some RCA skills the day we started receiving pink PCB assemblies! A while back, my job involved designing LED boards that were used to backlight colorfully silkscreened glass panels. Our engineering customers had specified the color of the PCBs to be white so as to enhance the reflectivity of the boards behind the glass. Anyone who has walked down the paint aisle of Home Depot will quickly realize that there are many shades and hues of white. But to keep things simple on our PCB fabrication drawing notes, the solder resist color was specified as "white."

Depending on the supplier of the bare PCBs, I had noticed various shade or hue differences from part number to part number. Sometimes the hue would be slanted toward gray. Sometimes the color would be shifted to a tan we called "toasted almond." Every so often, the hue would be slightly pinkish, which we referred to as "mauve." But for the most part, our many various PCB designs requiring white solder resist would pass incoming inspection because they were, well, "white-ish."

All seemed fine until our department's new purchasing clerk arrived and placed a new order for white PCB assemblies. Upon receipt, the box was opened and our entire design group heard the exclamation: "These boards are not white—these boards are pink!" Within a 48-hour period, the purchasing clerk had drafted a list of several possible suspects and organizations to blame. This new "problem," which was never identified as a problem previously, had been identified by a fresh set of eyes. The drama began to attract the attention of many others in the department, each with his own hypothesis on why the board assemblies were pink. Bare board suppliers were suddenly calling designers and describing how they were being accused of using pink solder resist by our purchasing depart-



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pink photo was included and labelled a “non-conforming” example. This was a critical step in defining the problem.

Second, we sought out all of the process stakeholders and brought them together to collect facts and to understand their materials and processes.

What we learned by communicating with all of the stakeholders was monumental. No one was conspiring to accept PCBs by buying them off in incoming inspection. No one was inanely applying pink solder resist to the PCB. After asking all the right people every possible question, we learned that a bare board supplier sought to overachieve with regard to our reflective “white” requirement. They ordered a new reflective white solder resist from their supplier. The new product was as white as one could imagine. It was applied to the PCB and covered with a beautifully, opaque, silky white finish. The PCBs were shipped to the assembly suppliers and were received, passing the “white” inspection point on the fabrication drawing with ease.

But surprisingly, after the bare PCB’s gold contact lands were coated with RoHS solder paste and run into the reflow oven environment, the white solder resist reacted to the temperatures and chemistry combination and turned the solder resist to pink! Then, the pinkish board assemblies moved on to inspection. There was no solder resist color requirement listed on the assembly inspection document. There was no reason to reject the PCB assemblies, so they were shipped. Nobody saw how the problem developed until being informed by using some elementary RCA processes. In the end, it turned out that the solder resist supplier had been experimenting with some chemical elements in the formula to increase opacity and improve reflectivity. During a perfect storm of compounds, chemistry and temperatures, voilà—pink PCBs. How much money was wasted? How much time was wasted? Who’s at fault here? Hopefully, we’ve learned that stuff happens. It’s how effectively we address it that matters, so it won’t happen again.

What else can PCB designers learn from RCA?

ment. The assembly supplier was re-directing PCB orders away from the present supplier in hopes of doing business with a bare board supplier who knew the difference between white vs. pink. It started getting personal. Stakeholders were reacting rather than responding.

To make a long story short, after several weeks, a wise manager stepped in and began asking questions. He asked if anyone were conducting any root cause analysis on this issue. He described the use of pareto charts and fishbone diagrams in a very constructive way. By simply asking questions, he helped the department to realize that they were merely spit-balling conspiracy theories and accusations. The department had been quick to find fault and place blame rather than getting to the real root cause of the problem. In a few more weeks, amazingly, this talented manager had changed the culture of the department enough so that we could focus on finding the root cause of our fancy pink PCB assemblies. To our surprise, the root cause was something none of us could have expected.

Here’s how it went down.

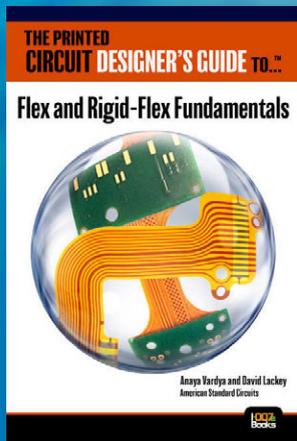
First, our engineering customers had to come up with some acceptability criteria to define a range of white. We follow the examples of the IPC acceptability specs IPC-A-600 and IPC-A-610, and we photographed a range of acceptability. A white photo was designated the “target condition.” Then, slightly tinted condition photos were noted as “acceptable” and lastly, a

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The engineering community is an interesting breed. Sometimes we experience the diva complex when things are going well in the design cockpit. We send our designs off to our manufacturing counterparts with high expectations. But why is it that when problems arise, we are so quick to switch suppliers or to issue that corrective action report? “Wham! Take that! And tell me how you’re going to keep it from happening again!”

We in the engineering and design community must realize that we are at the hub of the PCB information wheel. We need to understand that all of our data must be interpreted, and if it is not clear, it is prone to error. It’s an interesting point to ponder. What happens when the source of the problem is determined to be PEBCAK (Problem Exists Between Chair and Keyboard)? Why don’t we hear about it in the form of a CAR from our customer or boss or the supplier?

Yes, it’s hard to admit it, but there are times when designers make mistakes too. What should happen at that rare time when a designer points the manufacturing finger at a PCB problem and sees there are three design fingers pointing back? Rather than playing Led Zeppelin’s “Nobody’s Fault but Mine” over and over for everyone to hear, it is time to think about the root cause of your design failure.

“Sheesh! How’d that happen?” No, that’s never an acceptable response. An experienced PCB designer will know the importance of quickly getting to the root cause of a problem by examining the design process—yes, a documented, formal process. Does your design pro-

cess include design rule checking? Of course. But automatic design rule checking doesn’t check for everything. It won’t check your solder mask color. It won’t check your legend color either. Do you always check your dimensions, tolerances and next assembly fit? Probably not.

There are many other examples. A wise designer will solicit a design review from associated PCB project stakeholders and formulate a dynamic design checklist, adding to it each time a design problem is found. PCB stakeholder relationships are only torn down by assigning fault and blame. Industry relationships grow, however, when stakeholders work together to find the cause of a problem and correctly address the process it relates to, in order to prevent it from happening again.

Let’s stop pointing the fickle finger of fault when there’s a misstep or miscue. We’ll all be better off if we concentrate on ensuring that it never happens again. **PCBDESIGN**

### References

1. *Root Cause Analysis: A Tool for Total Quality Management*, by Paul F. Wilson, Larry D. Dell, and Gaylord F. Anderson, 1993.



**Kelly Dack, CID+**, is a PCB designer for a contract manufacturer in the Pacific Northwest. Additionally, Kelly serves on the executive staff of the IPC Designer Council and is employed by EPTAC Corporation as a CID instructor teaching classes nationwide.

## Neon FIB Solves Loss Issue in Superconducting Nanowire Devices

In a paper published in *Physical Review Applied* in July 2017, researchers at the London Centre for Nanotechnology, led by Dr Jon Fenton, have demonstrated the incorporation of superconducting nanowires within high-quality niobium nitride resonators. These nanowires were fabricated by neon focussed-ion-beam milling. Using an inert-gas ion-beam allows fabrication of constrictions as small as 20nm while introducing minimal levels of the two-level systems which contribute to loss.

Careful studies of the losses from these resonators have allowed the team to conclude that these resonators have quality factors better than 200000 in the low-temperature, single-photon limit relevant for quantum circuits. This is approximately 100× larger than equivalent resonators with embedded nanowires and compares favourably with the mature technology of AlOx-based Josephson junctions.

These results suggest that there are excellent prospects for superconducting-nanowire-based quantum circuits.

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# It Really Wasn't My Fault!

by **Tim Haag**

CONSULTANT

Everyone in my house is a baseball fan. Well, everyone but me, that is. I'm not saying that I dislike baseball; I enjoy watching a good game from time to time. But I don't sit around and watch it as much as the other members of my family.

The nearest professional team to my home in Portland is the Seattle Mariners. My brother-in-law is a fan, and my mother-in-law, my brother and his family, and my sons are all fans. But the most devoted fan of all is probably my wife. She knows the stats and trivia of the different players, and she knows the game well. I would rather watch something else with space-ships or explosions (or both), but the rest of the family wants baseball. And so, in the spirit of democracy, where the majority rules, baseball is what we watch.

Some years back, the Mariners had a designated hitter named Edgar Martinez. Edgar, if you don't already know, was one heck of a hitter. He won all kinds of awards, saved the day

on many occasions, and was a huge fan favorite. My family would hang on his every appearance at bat. The only problem is that whenever I watched, he would strike out. I started making a joke about it, saying, "That Edgar guy sure isn't much of a hitter."

I didn't believe what I was saying, mind you; I just said it to irritate my family. (What, you've never done that?) This routine went on for some time. I kid you not; every time I watched Edgar at bat, he would strike out. Finally, it got to the tipping point; once again Edgar was up to bat and I came in the room to watch. To my astonishment, my entire family screamed at me to get out of the room, and they weren't kidding. They were putting the blame on me for his past strikeouts, and they kicked me out to give him the best opportunity to hit.

It really wasn't my fault.

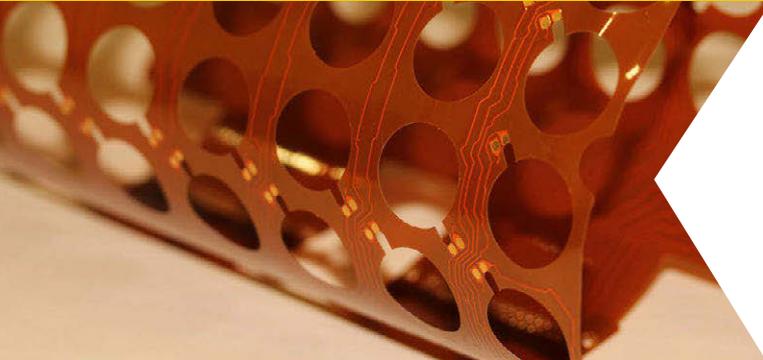
That is an amusing example of getting blamed for something that isn't your fault, and that story has been told repeatedly in Haag fam-



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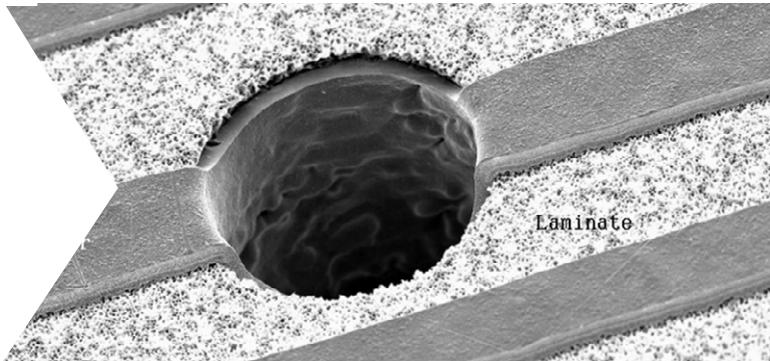
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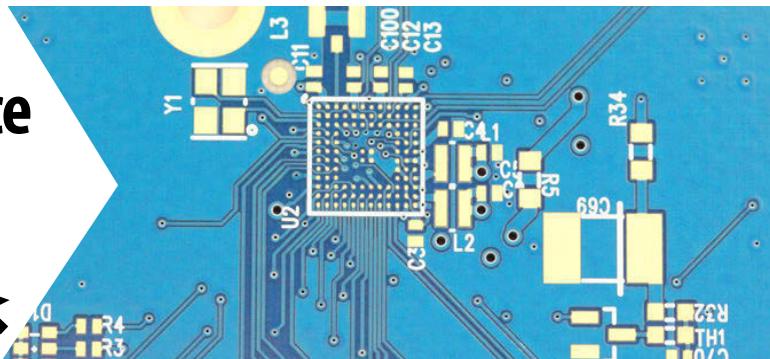
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ily lore. But most of the time, being blamed for something that wasn't your fault is not nearly so funny, and in the work realm it can be downright disastrous.

Back when I designed boards for a computer manufacturer, I once received verbal instructions from an engineer who directed me to make a certain change. I completed this change and didn't think another thing of it. Many months later, this same engineer told me in a serious conversation that there were troubles with the board and all its successive versions because of the change that I had made. I told him that this was the change that he had requested, and I figured that would end the discussion because my word is my bond. But he stood his ground and even suggested that my job was on the line because of all the scrap boards that had resulted from this error.

“ I sweated bullets on this issue. I reviewed it in my mind and went back and forth trying to remember as many details that I could to bolster my defense. ”

I sweated bullets on this issue. I reviewed it in my mind and went back and forth trying to remember as many details that I could to bolster my defense. I looked in vain for any kind of evidence to back up my actions, but since it was a verbal request there wasn't anything available. I kept expecting the hammer to drop on me any day, and a couple of months went by without me knowing what my fate would be. Finally, I went back to the engineer and asked him whatever had become of this problem. He told me not to worry, that he had gone back through his records and found the original data that had driven his verbal request and that I had been off the hook now for quite some time. I meekly thanked him and left his office without giving

him a piece of my mind for keeping me in suspense for so long.

So, in hindsight, what could I have done to save myself a couple of months of suspense and worry? The truth is that misunderstandings are always going to happen, and unfortunately bad things do seem to happen to good people. But here are some ideas for things we can do to help reduce these conflicts.

First, do your best to build trust into your work relationships. In my experience people are the least communicative when they feel that they have to protect themselves. Those who feel a need to protect themselves usually keep important data and information close to the vest so that they can either prove their value if they feel threatened or keep ammunition in their pocket for a rainy day. If this sounds completely alien to you, then congratulations; you must be working in an environment where trust is thriving. But sadly, there are many dysfunctional organizations out there where workers have learned the hard way that in order to survive, they need to arm themselves with anything they can, including relevant data that should be general knowledge.

On the other hand, when people trust those that they work with, those are the relationships that enjoy the best communication and information is openly shared. So, if you are in an environment where trust is minimal, take a risk and start investing trust in your fellow employees. When you show people that they can rely on you, they will often reciprocate and a healthier work relationship based on trust will begin to grow.

Second, stick to the established design process. If you don't have a regular design process in place, then work with your managers and coworkers to create one. Every design department that I have worked in has had some sort of control change process. In the story that I related earlier, there was a control change process in place—I just didn't use it. In fact, I completely ignored it. I got a verbal request from the engineer in charge and instead of following the process, I just did what he asked without thinking about it.

I realize that this is a very touchy point. You need to be flexible enough to handle changes

# ROG breaks FR-4 barrier!

Introducing  
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## Need Better RF Performance? FR-4 No More!

Demand for wireless data is growing exponentially, driving a need for substantially higher levels of mobile network capacity and performance. This demand will grow further in support of the upcoming 5G IoT ecosystem where



billions of devices will be communicating with each other, and connectivity is immediate and uninterrupted. FR-4 was historically a material choice for many less demanding RF applications, but changes in the wireless infrastructure related to growing performance requirements, especially in small cells and carrier-grade WiFi/Licensed Assisted Access (LAA), have resulted in instances where the properties of FR-4 are lacking, and RF performance and consistency is compromised. There's no longer a need to sacrifice your PCB performance.

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and yet regulated enough to protect against confusion. And since the board design process usually involves a lot of time spent with different engineers you will have to decide what interaction constitutes standard design input, and what interaction becomes a change that requires process control.

And lastly, make sure that you document your work. I'm not talking about documenting your fellow employees here, that kind of thing completely ruins the trust that you are already trying to build. No, I'm talking about keeping organized documentation of the work that you are doing. If I had kept a record of the changes that I had been requested to do I could have easily shown the engineer on what day he requested me to make the change, why the request had been made, and how I accomplished the task.

There are several ways to accomplish better documentation. One would be to keep electronic or hard copies of formal requests like engineering change orders, etc. Another would be to keep a personal journal, or log, for the job that you are working on. In some design departments that I've worked in, the "job log" is automated and part of the actual design. I know that this sounds like a lot to do, but you don't have

to make a mountain out of a mole hill here. Electronic copies can easily be made, and adding a sentence to a Word document or a spreadsheet is very simple. The key is to get organized and then stick to that organization consistently.

I hope that this helps, and I really wish that I had thought through all these things before I got the blame put on me. Sure, we can say that it really wasn't my fault, but saying that usually won't get us off the hook.

Make sure that you've built trust with your co-workers, that you are backed up by controlled processes, and that you can prove through documentation that what you're doing what is requested of you. In this way, you can help to make sure that it really wasn't your fault. And lastly, don't ever joke with my family about Edgar Martinez being a lousy hitter. I sure found that one out the hard way! **PCBDESIGN**



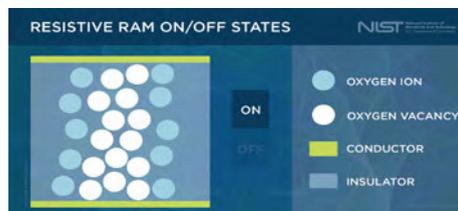
**Tim Haag** is a consultant based in Portland, Oregon.

## With a Gentle Touch, NIST Scientists Push Us Closer to Flash Memory Successor

Sometimes a light touch is best. Research at the National Institute of Standards and Technology (NIST) suggests this may be true in the microscopic world of computer memory, where a team of scientists may have found that subtlety solves some of the issues with a novel memory switch.

This technology, resistive random access memory (RRAM), could form the basis of a better kind of non-volatile computer memory, where data is retained even when the power is off. Flash technology has essentially reached its size and performance limits.

RRAM could surpass flash in many key respects: It is potentially faster and less energy-intensive. But RRAM has yet to be broadly commercialized because of technical hurdles that need addressing.



One hurdle is its variability. A practical memory switch needs two distinct states, representing either a one or a zero, and component designers need a predictable way to make the switch flip.

The NIST team decided to try a lighter touch—using less energetic pulses of 100 picoseconds, about a tenth as long. They found that sending a few of these gentler signals was useful for exploring the behavior of RRAM switches as well as for flipping them.

"Shorter pulses reduce the variability," Nminibapiel said. "The issue still exists, but if you tap the switch a few times with a lighter 'hammer,' you can move it gradually, while simultaneously giving you a way to check it each time to see if it flipped successfully."

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### [Weiner's World—June 2017](#)

On the return from Hong Kong last week I had the good fortune of meeting an officer of Allegro Microsystems and enjoyed a wide-ranging discussion with him. One of the “take home” items was concern about an expanding shortage of rare earth metals used to make ICs for the burgeoning automotive sensor market.

### [Mr. Laminate Tells All: PTFE is about to be Banned by IEC TC111](#)

Technical Committee 111 of the International Electrotechnical Commission (IEC) is preparing to effectively ban PTFE (polytetrafluoroethylene) materials from electronics. As history goes, the electronics industry has focused on only two of the four halogens (bromine and chlorine) to be limited to be called “halogen-free” or more accurately “low-halogen.”

### [EPTE Newsletter: Transparent Flex Circuits, Stretchable Flex Circuits](#)

Most of the products on display at the JPCA Show were related to electronics, the electronics industry, packaging and electronic circuits. Flex circuit manufacture and material companies that featured flexible circuits at the exhibition focused their attention on transparent flex circuits and stretchable flex circuits.

### [One World, One Industry: Three Ways to Close the Skills Gap in U.S. Manufacturing](#)

The skills gap is a chronic problem in the manufacturing sector. Most manufacturing companies have a hard time aligning the talent needed to run their businesses with the talent that is available to work locally. And as new innovations emerge, new skills requirements emerge as well.

### [All About Flex: Etchback on Type 3 and Type 4 Flexible Circuits](#)

Through-hole etchback is a requirement that is sometimes specified on medical, military and aerospace procurement documents for multilayer flexible circuits and combination multilayer flex/rigid board circuits. It specifically relates to the copper plated through-holes and the relative dimensions between the dielectric layers and copper layers.

### [Happy's Essential Skills: Tip of the Month—The NIST/SEMATECH e-Handbook of Statistical Methods](#)

In the 1990s, the National Bureau of Standards was distributing a popular statistical document, Handbook 91. A request by Patrick Spagon of the Statistical Methods Group of SEMATECH to update the NBS Handbook 91, Experimental Statistics, has resulted in a new web-based statistical handbook including statistical software.

### [The Significance of the PCB in the Value Chain of the European EMS Industry](#)

At SMT Nuremberg, Pete Starkey meets with Dieter Weiss, who comments upon the significance of the PCB in the value chain of the European EMS industry, and looks to a future where we embrace an open-minded attitude and a willingness to work together.

### [Megasonic Acoustic Surface Treatment Process for Enhanced Copper Electrodeposition in Via Interconnects](#)

A printed circuit board is populated with a multitude of electro-mechanical components plus various active and passive devices such as transistors, capacitors, inductors and resistors, which enable the functionality and assembly of the PCB.

### [Review of the 2017 IPC Reliability Forum](#)

IPC continues to lead our industry by example with their inaugural Reliability Forum, held in Chicago in April. The event was focused on manufacturing high-performance products and featured industry royalty from both a speaker and audience standpoint.

### [Jill Scadden Joins Advanced Circuits as Business Development Manager](#)

Advanced Circuits welcomes Jill Scadden as business development manager. She will be responsible for discovering new business opportunities and enhancing Advanced Circuits' offerings by working closely with customers and prospects to create customized solutions for their unique PCB fabrication needs.

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# When Legacy Products No Longer Perform

by Barry Olney

IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

As IC die sizes continue to compact due to demand for smaller and faster technology, and as switching speeds continue to improve, rise and fall times are creeping down into the sub-nanosecond realm, a territory previously reserved for microwave engineers. This relentless shrinking trend that perpetuates Moore's Law can create a huge problem for legacy designs as faster switching intensifies signal integrity issues. Over the years, as logic drivers have continued to switch faster and faster, problems with ringing, crosstalk and electromagnetic emissions (EMI) have become progressively worse.

It is a common quandary that established products that have worked flawlessly for years suddenly stop performing reliably, due to a new batch of ICs that is used in the latest production run. The cause of this problem is rise time shrinkage. Figure 1 illustrates the consequences of three different rise times for the same clock frequency.

This example brings home two very important points. Firstly, for a given layout, faster switching produces spurious signals exhibiting excessive overshoot and ringing. This problem is unavoidable. It can only be prevented,

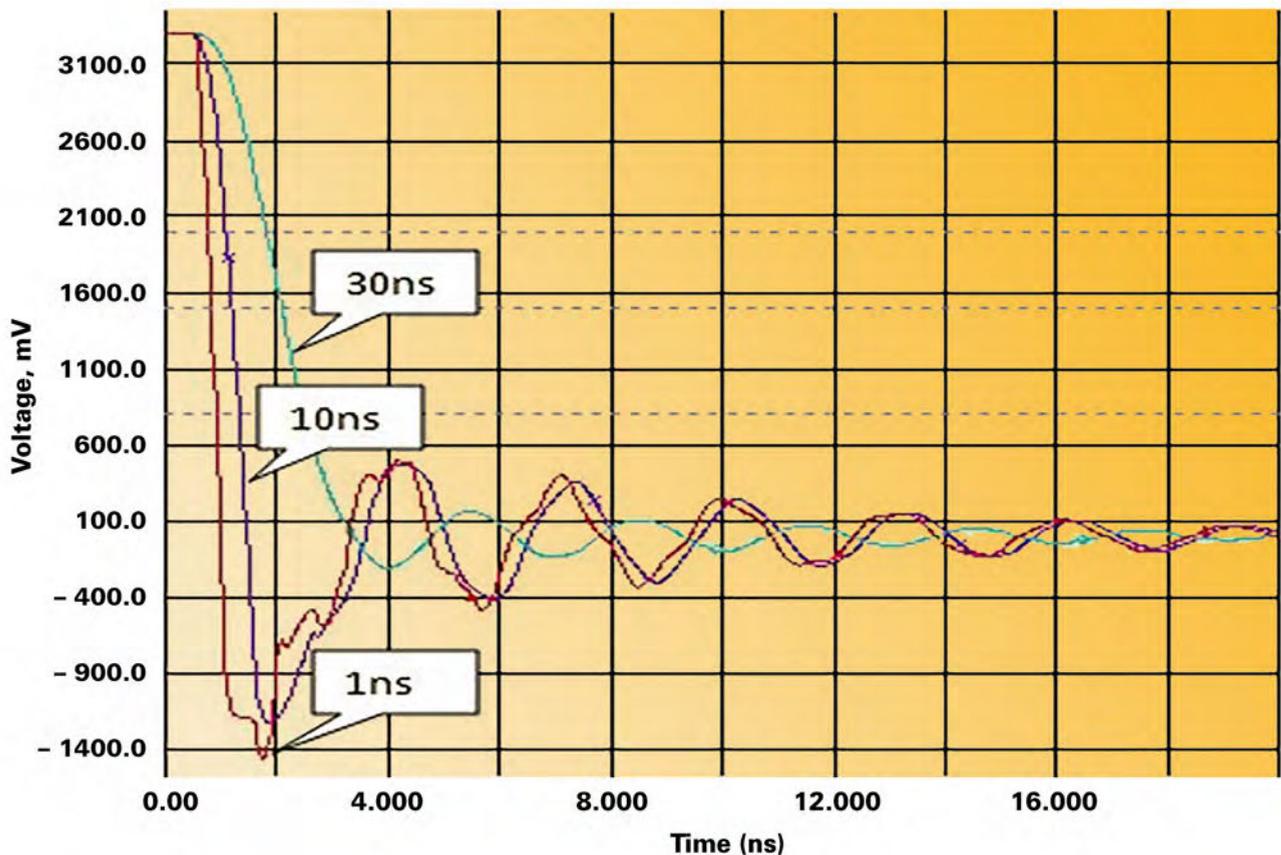
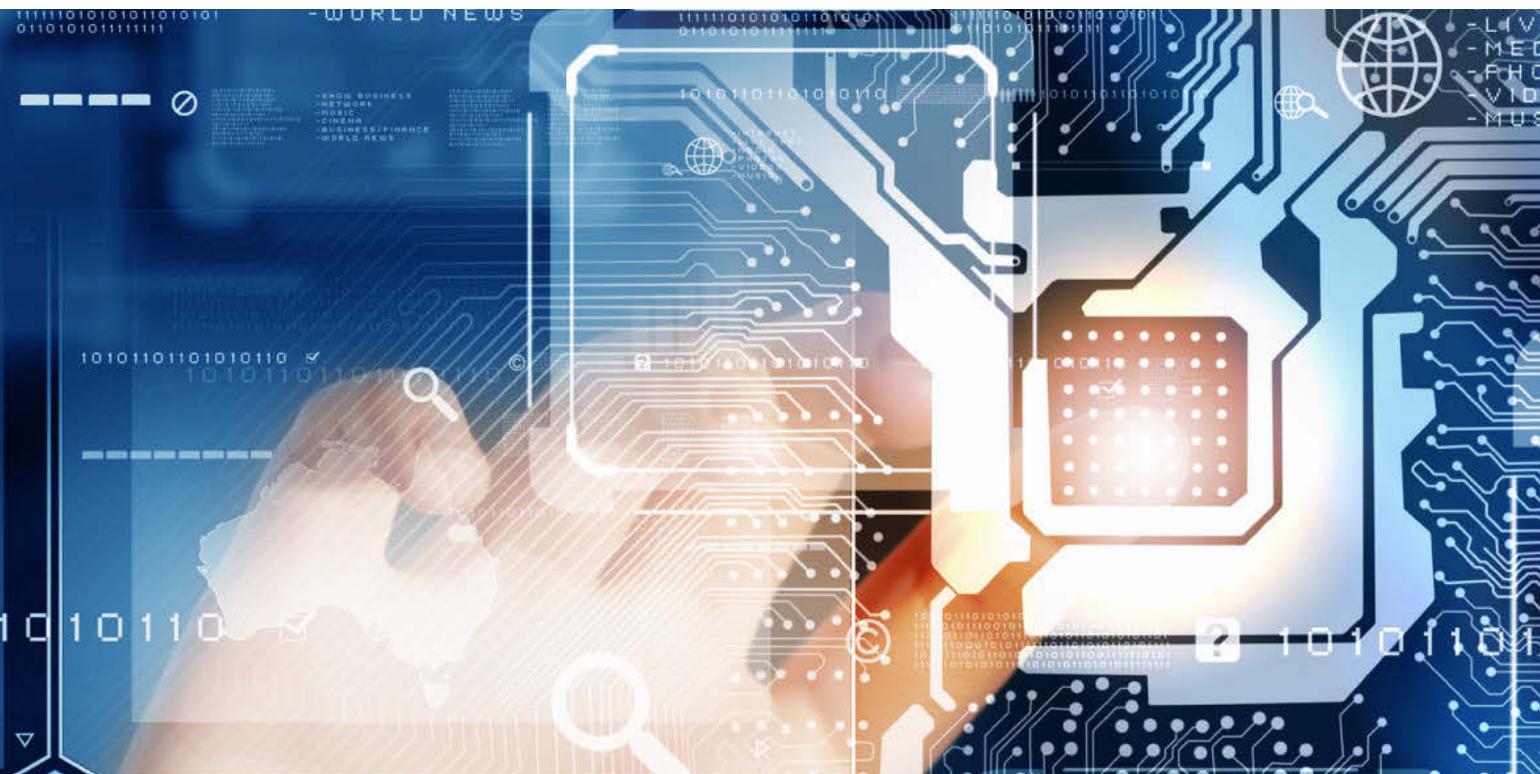


Figure 1: Increased ringing with faster rise times (simulated in HyperLynx).

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to some extent, by improving the layout and routing, reducing the number of loads and/or adding terminators. Secondly, IC manufacturers are not always doing us a favor when they begin shipping “new and improved” logic circuits. When substituted into a legacy design, the increase in speed may buy nothing but headaches.

From the perspective of an IC manufacturer, shrinking a die is a winning proposition because the new chip is almost certain to meet or exceed its published specifications at a lower cost. However, from the perspective of the designer, shrinking a die, in an existing product design, can be a daunting prospect, because the new rising and falling edges are almost certain to switch considerably faster.

Faster edge rates mean reflections and signal quality problems. So, even when the package hasn’t changed and the clock speed hasn’t changed, a problem may exist for legacy designs. The enhancements in driver edge rates have a significant impact on signal quality, timing and crosstalk. This also has a direct impact on radiated emissions.

Figure 2 shows the massive increase in emissions from the slowest to the fastest rise time previously discussed. When dealing with subnanosecond rise times, the emissions can easily exceed the FCC/CISPR Class B limits for an unterminated transmission line.

The ratio of signal rise time to physical delay of an interconnect determines how the circuit behaves. A small ratio, meaning a short

rise time compared with the innate time delay of the interconnect, produces distributed behavior. Whereas a large ratio invokes lumped-element behavior that requires little attention. When considering any aspect of your circuit geometry, the relationship between physical size and rise time determines the relative importance of that object in the overall scheme of the circuit. The signal rise time, rather than the signal clock frequency, determines the critical signal speed. Basically, any rise time of 1ns or less may be of concern.

An ideal square wave clock signal with the spectrum of a 50% duty cycle, and a zero picosecond rise time, has frequency components (harmonics) only at multiples of the clock frequency. The Fourier Transform converts a time domain waveform into its spectrum of sine wave frequency components. The amplitude of the even harmonics is zero, as they cancel out in the Fourier Transform due to the even mark-to-space ratio. The amplitude of the odd harmonics is given by:

$$V (\text{harmonics}) = \frac{2}{\pi \cdot n}$$

where n is the odd harmonic number

For example, the amplitude of the 1<sup>st</sup> harmonic, where n = 1, is 2/(3.14 x 1) = 0.64V. The amplitude of the 3<sup>rd</sup> harmonic, n = 3 is 2/(3.14 x 3) = 0.21V. The amplitude of each harmonic

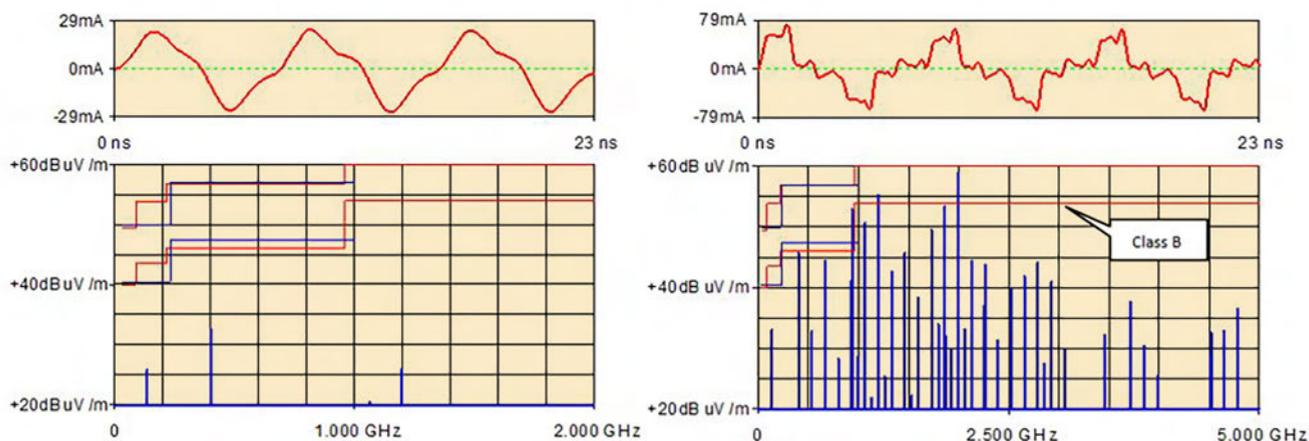


Figure 2: Radiated emissions from the 30ns edge rate (left) and 1ns (right).

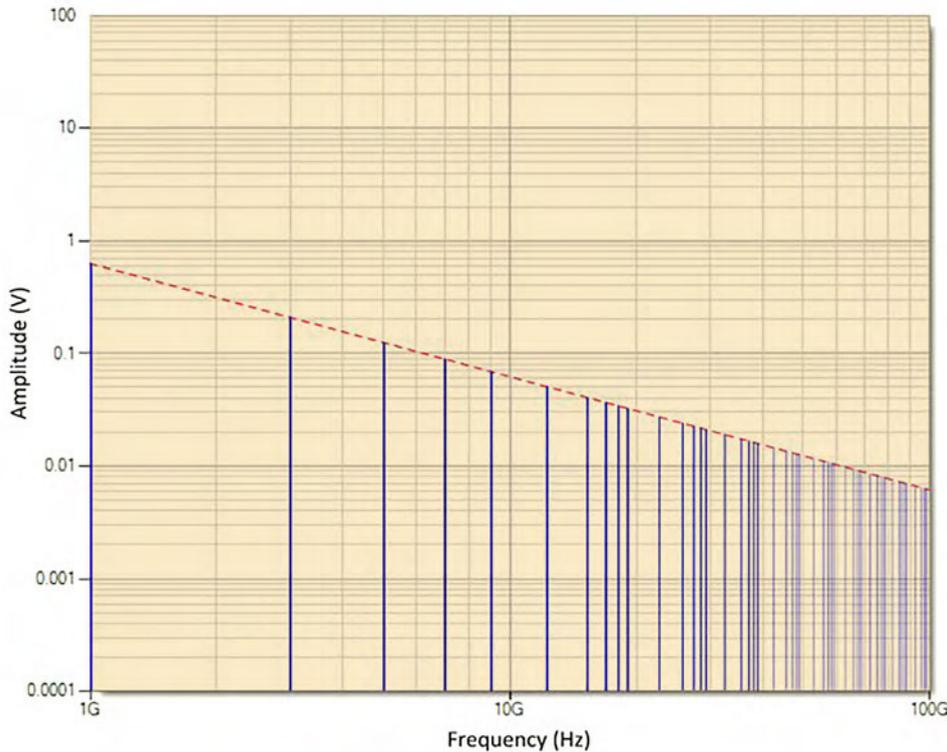


Figure 3: Odd harmonics of a 1GHz fundament clock.

drops off with the inverse of frequency, since each harmonic is a higher frequency. Figure 3 shows the calculated harmonic amplitudes of an ideal 1GHz clock signal for the odd harmonics up to 100GHz.

However, in practice, the signal rise time has an impact on the maximum signal bandwidth. Understanding the frequency band, that really matters, for digital design is very important. Traditionally, we used  $0.35/\text{Tr}$  (where  $\text{Tr}$  is the rise time in ps) for the upper bandwidth. However, a more accurate approach is to use an upper knee frequency of  $0.5/\text{Tr}$ , which forms a crude but useful translation between time and frequency domains. If, for instance, the rise time is 500ps, which is typical these days, then the upper bandwidth is actually 1GHz regardless of the clock frequency. It is possible to have two different waveforms, with exactly the same clock frequency but different rise times and therefore different bandwidths.

When selecting the most appropriate dielectric materials for a design, one should consider the bandwidth up to the 5<sup>th</sup> harmonic. The bandwidth of an interconnect refers to the high-

est sine wave frequency that can be transmitted by the interconnect without significant loss. For our 1GHz example, the maximum bandwidth to consider is the 5<sup>th</sup> harmonic at 5GHz if the rise time is unknown.

FR-4, the glass epoxy material commonly used for multilayer printed circuit fabrication, has negligible loss at frequencies below 1GHz. But since the dielectric loss is frequency-dependent, at higher frequencies, the dielectric loss of FR-4 increases. So, for high-frequency digital, RF and microwave designs, alternative materials that exhibit lower losses need to be considered. (To

make this selection process easier, over 31,000 rigid and flexible materials, up to 100GHz, can be sourced from the iCD dielectric materials library.)

Electromagnetic emissions arise from each frequency component of the signal. For the worse offender—the common-mode currents—the amount of radiated emissions will increase linearly with frequency. Although the amplitude of each harmonic drops off with the inverse of frequency, the ability to radiate increases linearly, so all harmonics contribute equally to EMI. To minimize EMI, the design goal is to use the absolute lowest bandwidth possible whilst still maintaining the specified data throughput.

Any ringing in the circuit may increase the amplitude of higher-frequency components and thus increase the magnitude of radiated emissions. High-frequency harmonics can also beat with the resonant frequency of the plane pairs, as they approach half wave length, creating a rough wave effect which, in extreme cases, can cause total system failure. This is the reason why solving signal integrity issues is always the best starting place to minimizing EMI.

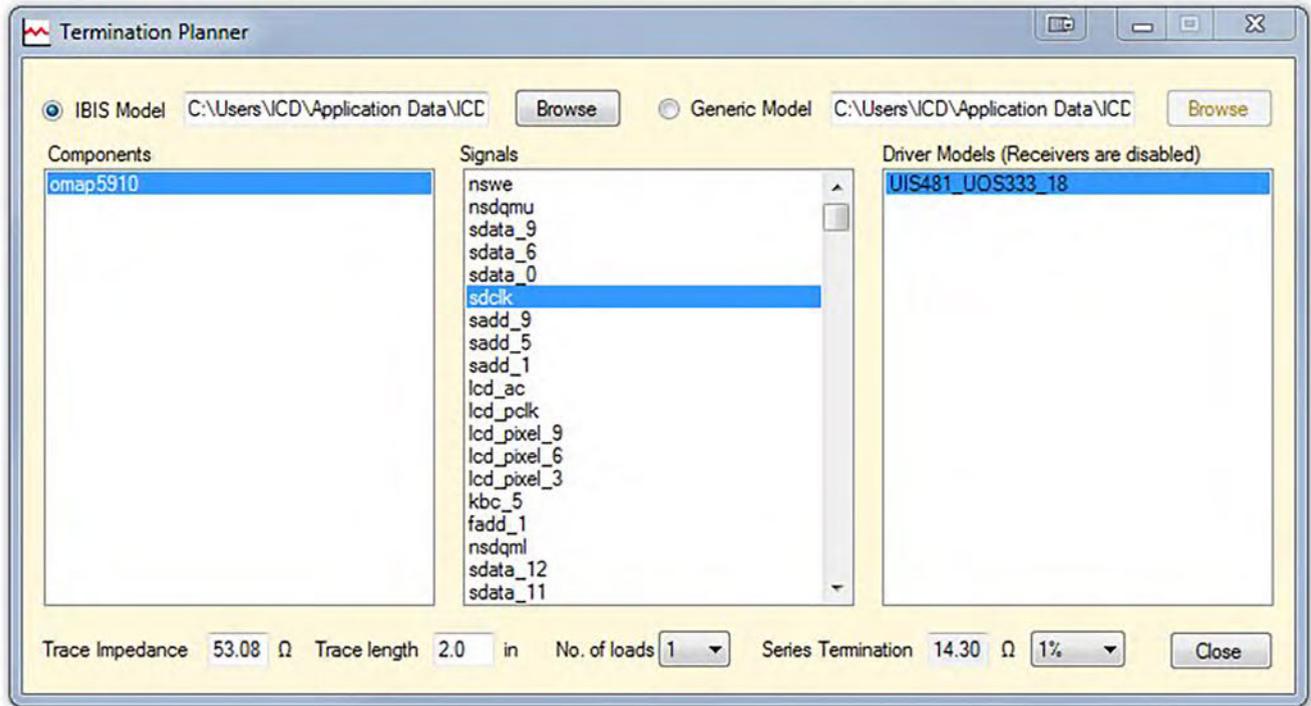


Figure 4: Series terminator value determined for an FPGA clock (source: iCD Design Integrity).

To improve signal integrity, hence EMI, one needs to slow down the rise time of the signal to reduce the high-frequency components. This is easily achieved by placing a termination resistor in series with the transmission line at the source. The value of this terminator is determined by extracting the IV curves from the IC IBIS model, and then the required series termination resistance is calculated, based on a distributed system, to match the transmission line for the selected layer as shown in Figure 4. So, to fix that legacy product that now exhibits intermittent operation, simply add a series terminator. In fact, it is always good design practice to allow space for a series terminator by adding a zero-ohm resistor to the critical interconnects to future-proof the design.

**Points to Remember:**

- Faster switching intensifies signal integrity issues by producing spurious signals exhibiting excessive overshoot and ringing. This also has a direct impact on radiated emissions.
- Established products can suddenly stop performing reliably due to a new batch of ICs. The cause of this problem is rise time shrinkage.

- Even when the package hasn't changed and the clock speed hasn't changed, a problem may exist for legacy designs.
  - The emissions from sub-nanosecond rise times, can easily exceed the FCC/CISPR Class B limits for an unterminated transmission line.
  - The ratio of signal rise time to physical delay, of an interconnect, determines how the circuit behaves.
    - An ideal square wave clock signal has frequency components only at odd multiples of the clock frequency.
    - In practice, the signal rise time has an impact on the maximum signal bandwidth.
    - The upper knee frequency of  $0.5/T_r$ , forms a translation between time and frequency domains.
    - When selecting the most appropriate dielectric materials for a design, one should consider the bandwidth up to the 5<sup>th</sup> harmonic.
    - For high-frequency digital, RF and microwave design alternative materials that exhibit lower losses need to be considered.
    - Although the amplitude of each harmonic drops off with the inverse of frequency, the ability to radiate increases linearly—so all harmonics contribute equally to EMI.



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- High-frequency harmonics can beat with the resonant frequency of the plane pairs creating a rough wave effect which can cause total system failure
- Solving signal integrity issues is always the best starting place to minimizing EMI.
- To improve signal integrity, hence EMI, one needs to slow down the rise time of the signal to reduce the high-frequency components. This is easily achieved by placing a termination resistor in series with the transmission line at the source.
- It is always good design practice to allow space for a series terminator by adding a zero-ohm resistor to the critical interconnects to future-proof the design. **PCBDESIGN**

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2. Eric Bogatin, Signal and Power Integrity Simplified, [Rule of Thumb #1: Bandwidth of a signal from its rise time](#).

3. Howard Johnson, Martin Graham. [High-speed Digital Design](#).



**Barry Olney** is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD

Stackup, PDN and CPW Planner. The software can be downloaded from [www.icd.com.au](http://www.icd.com.au). To read past columns, [click here](#).

## Simultaneous Design and Nanomanufacturing Speeds Up Fabrication

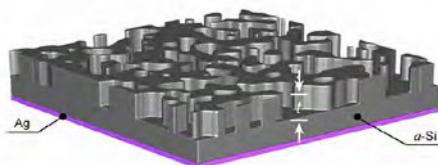
Design and nanomanufacturing have collided inside a Northwestern University laboratory.

An interdisciplinary team of researchers has used mathematics and machine learning to design an optimal material for light management in solar cells, then fabricated the nanostructured surfaces simultaneously with a new nanomanufacturing technique.

"We have bridged the gap between design and nanomanufacturing," said Wei Chen, the Wilson-Cook Professor in Engineering Design and professor of mechanical engineering in Northwestern's McCormick School of Engineering.

"The concurrent design and processing of nanostructures paves the way to avoid trial-and-error manufacturing, increasing the cost effectiveness to prototype nanophotonic devices," said Teri Odom, Charles E. and Emma H. Morrison Professor of Chemistry in Northwestern's Weinberg College of Arts and Sciences.

Researchers are currently interested in nanophotonic materials for light absorption in ultrathin, flexible solar cells. The same



principle could also be applied to implement color into clothing without dyes and to create anti-wet surfaces. For solar cells, the ideal nanostructure surface features quasi-random structures, meaning the structures appear random but do have a pattern.

To bypass the issues of nano-lithography, Odom and Chen manufactured the quasi-random structures with wrinkle lithography, a new nanomanufacturing technique that can rapidly transfer wrinkle patterns into different materials to realize a nearly unlimited number of quasi-random nanostructures.

"Importantly, the complex geometries can be described computationally with only three parameters — instead of thousands typically required by other approaches," Odom said. "We then used the digital designs in an iterative search loop to determine the optimal nanowrinkles for a desired outcome."

Next, the team plans to apply its method to other materials, such as polymers, metals, and oxides, for other photonics applications.



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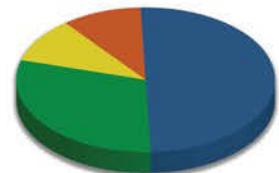
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# MilAero007 Highlights



## [First-Ever Helicopter-Based Firing of High Energy Laser](#)

Raytheon Company and the U.S. Army Apache Program Management Office, in collaboration with U.S. Special Operations Command, recently completed a successful flight test of a high energy laser system onboard an Apache AH-64 at White Sands Missile Range, New Mexico.

## [All About Flex: Etchback on Type 3 and Type 4 Flexible Circuits](#)

Through-hole etchback is a requirement that is sometimes specified on medical, military and aerospace procurement documents for multilayer flexible circuits and combination multilayer flex/rigid board circuits. It specifically relates to the copper plated through-holes and the relative dimensions between the dielectric layers and copper layers.

## [Mil/Aero Electronics Supply Chain Facing New Challenges](#)

For this month's issues of I-Connect007 publications, we invited a sampling of professionals whose experience centers on the electronics industry in the military and aerospace world, including experts from design, PCB manufacturing, and the assembly arena, to sit down with us for a frank discussion. Our discussion centered on the challenges associated with military work, including the new regulatory requirements for cybersecurity, dealing with leaded vs. lead-free components, and the differences and similarities with the commercial world.

## [PNC Inc. Invests in LED Laser Direct Imaging system from Miva Technologies](#)

This 2000L 2LE model is capable of imaging a maximum size 24" x 24" PC board or film size. With any large format film, positional accuracy can be a challenge but the Miva's dynamic scaling feature can increase accuracy to minimize tolerance build-ups during the imaging process.

## [A.I. Will Prepare Robots for the Unknown](#)

"The goal is for A.I. to be more like a smart assistant collaborating with the scientist and less like programming assembly code," said Chien, a senior research scientist on autonomous space sys-

tems. "It allows scientists to focus on the 'thinking' things—analyzing and interpreting data—while robotic explorers search out features of interest."

## [American Standard Circuits Promotes Tim Hudson to Flex, Rigid-Flex and Special Products Manager](#)

American Standard Circuits CEO Anaya Vardya has announced the promotion of industry expert Tim Hudson to the position of flex, rigid-flex and special products manager. Hudson was formerly the company's plant manager. During his 31-year career in the printed circuit board industry, he has held key positions with several companies including Midwest Printed Circuits, DEH and Bartlett.

## [Rockford Region Cultivates Opportunities at Paris Air Show](#)

More than a dozen aerospace organizations and companies promoted the strength of the Rockford Region's aerospace supply chain and pursued opportunities to expand their scope worldwide June 19–22 at the 52nd International Paris Air Show.

## [Greg Papandrew to Lead Advanced Circuits' Offshore Division](#)

Offshore PCB sourcing expert Greg Papandrew has been tapped as the offshore sales director for Advanced Circuits' newly created offshore division. Papandrew is responsible for creating a seamless process and providing the most cost-effective offshore manufacturing solution for high-volume PCB production to customers in the North American market.

## [Smart Quadcopters Find their Way without Human Help or GPS](#)

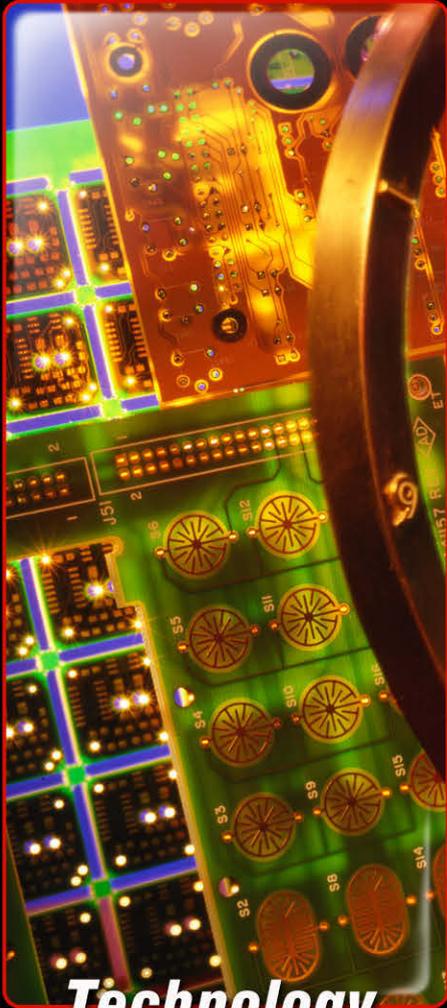
Milestone series of tests have quadcopters slalom through woodlands, swerving around obstacles in a hangar and reporting back to their starting point all by themselves.

## [Eltek Receives \\$1.4 Million Loan from Nistec](#)

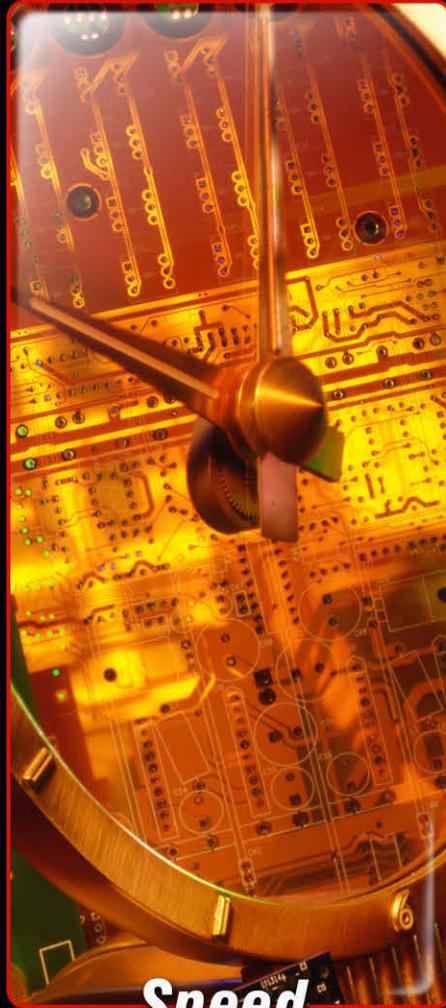
Eltek Ltd has obtained a loan of NIS 5 million (approximately US\$1.4 million) from Nistec Ltd, the company's controlling shareholder.

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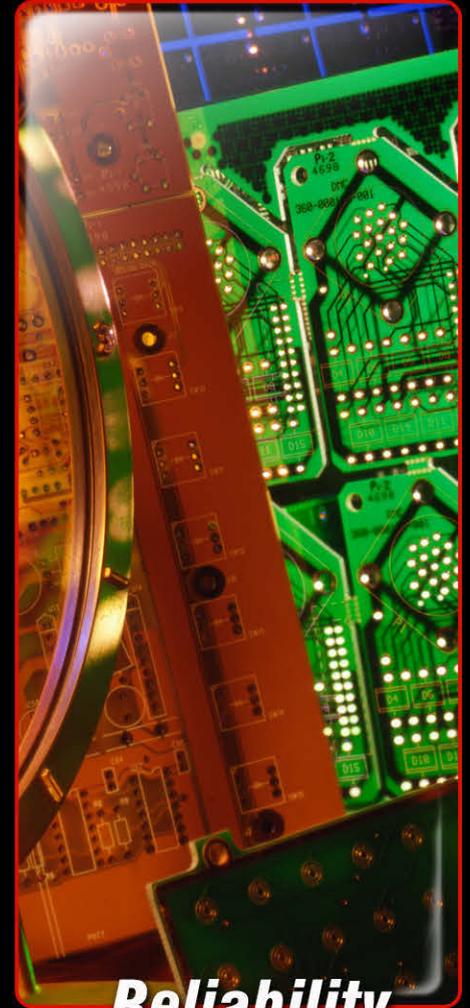
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# Thermal Management: The Heat is On

by Jade Bridges

ELECTROLUBE

For some months now, my colleague Alistair Little has been taking a close look at resins and their role in circuit protection across an array of applications. He now hands the reins over to me, and in this, the first of what I hope will be a series of informative columns, I am going to focus on the all-important subject of thermal management. First, though, let me introduce myself.

I've worked for Electrolube for 14 years now, starting as a development chemist, then as the research & development Manager working with the product development team. In 2011, I moved into a more commercial role, working alongside the sales team to help with technical enquiries and product application queries. Last year, I was appointed manager of Electrolube's Ashby-based technical support team, working alongside sales, marketing and the R&D teams to provide more in-depth product support for both existing and new customers.

Thermal management—the science and the products—is my specialty, so let's start this series of columns (as Alistair did for his series on resins) with a five-point guide based on some typical questions that our technical support team fields every day on the phone, at exhibitions and when visiting customers.

## Why use thermal management materials?

During use, some electronic components can generate significant amounts of heat. Failure to effectively dissipate this heat away from the component and the equipment in which it is installed can compromise reliability and reduce operational life. Thermal management materials are designed to prolong equipment life and reduce incidences of failure. They also maintain equipment performance parameters and reduce energy consumption by reducing operating temperatures, and minimising the risk of damage to surrounding components.



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Indirectly, they maintain brand reputation, as the reliability of the equipment will be very dependent upon the effectiveness of the thermal management technique used.

### **What choices are available with thermal management materials?**

These can take the form of a thermal paste, an adhesive, a room-temperature vulcanized (RTV) silicone, phase change material, a thermal gap pad, or some other thermally conductive medium, the choice of which will depend upon the application. Commonly used thermal interface materials, including pastes, RTVs and adhesives, are introduced via a thin layer of material between the component and its heatsink to minimise its thermal resistance.

Pastes are non-curing, allowing rework, and consist of thermally conductive fillers in a carrier fluid, the former being a blend of one or more mineral fillers depending on the desired thermal properties, and the latter a silicone or non-silicone based medium. RTVs and adhesives are used to bond the heat sink to the component while also offering an effective heat transfer medium.

.....

“ RTVs and adhesives are used to bond the heat sink to the component while also offering an effective heat transfer medium. ”

.....

Innovative new phase change materials offer several advantages over thermal pastes. Their low phase change temperature allows low thermal resistance over a wide temperature range, ensuring minimal bond line thickness with improved stability and pump out resistance when compared with a thermal paste.

Other methods include thermal gap filler pads, which can be silicone or non-silicone

based sheet materials that can be cut to size and applied by hand. They are highly thermally conductive, but have a higher thermal resistance when compared with thermal pastes due to the thickness of the gap pad versus the very low thickness achievable with a thermal paste

For certain types and designs of heat generating circuitry, it may be more beneficial to encapsulate the device in a heatsink enclosure using a thermally conductive encapsulation compound. This provides both heat dissipation and environmental protection all in one.

Electrolube's thermal management products are all non-electrically conductive, ensuring that there are no issues with electro-migration due to the transfer of electrically conductive particles.

### **Why is resistance to thermal cycling important with thermal management?**

Thermal cycling (alternate heating and cooling) happens with the majority of applications that require a thermal management material. Non-curing products offer the lowest thermal resistance as they allow for a very low bond line thickness. However, they do suffer from pump-out, which occurs when differences in the coefficient of thermal expansion cause a non-curing product to move at the interface. This can lead to uneven coverage and therefore an increase in thermal resistance. Hotspots may form and at worst, the thermal interface material may be 'pumped out' of the interface. A thin, even coverage is needed throughout the life of the product, so the more stable the thermal interface material is to thermal cycling, the more consistent will be its heat transfer properties.

### **Are all thermal management materials suitable for manual or automated application?**

Except for thermal gap pads, which can be difficult to place automatically, most thermal management materials can be both manually and automatically applied (though manual is more likely in the case of prototyping/small production runs). Whether manual or automatic, the aim is to achieve a thin, uniform layer. Screen printing and application with a syringe can be achieved manually or automatically, but

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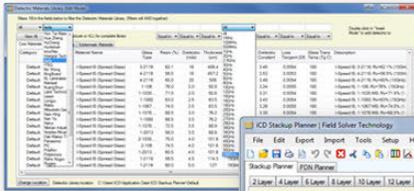
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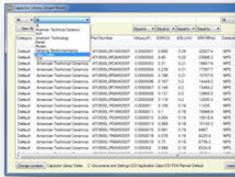
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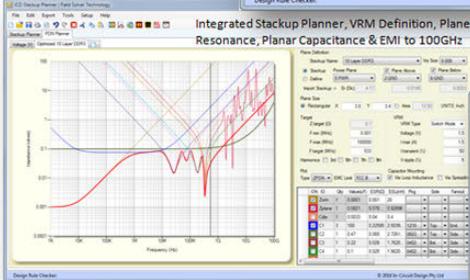
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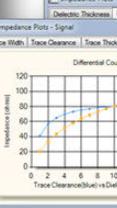
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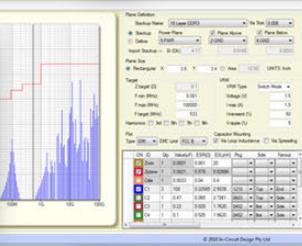


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it is important to get the dosage right and avoid the need to remove excess material.

What would be your top tips for deciding on the best material for an individual application?

For an interface material, the bond line thickness needs to be as thin as possible to minimise thermal resistance. For a gap filling material, the dimensions of the gap need to be considered and the conditions of use evaluated to decide whether a curing or non-curing product would be best in terms of the physical stability of the material and the ability for it to stay in place.

In all cases, the operating temperature range and environmental conditions of the application need to be reviewed. If very high temperatures are expected, a silicone may be required, and if the assembly is subject to rework, then a non-bonding, non-curing product should be used. If thermal protection is localised to one component, a curing product is the better choice as it will avoid migration of the material to neighbouring components.

There's a lot to consider when choosing a thermal management material; getting it wrong could compromise the reliability of an electronic assembly and shorten its life expectancy. It's strongly advisable to do your calculations, consider the equipment's operational and environmental conditions and experiment – but first and foremost, seek some expert advice as there are thermal management materials which might solve your requirements more sufficiently. I hope this first column has been useful and of course, we are always happy to help and offer advice. In the meantime, look out for my column on thermal management, which will appear next month. **PCBDESIGN**



**Jade Bridges** is the global technical support manager for Electrolube Ltd.

## Before, it was 3D Printing: Now Additive Manufacturing is the New Black

Places were in high demand for the Additive Manufacturing conference, which was held for Danish manufacturing companies in spring 2017. Additive manufacturing covers manufacturing technologies that involve building up components in layers by depositing material. This can be done by means of several different methods, one of them being 3D printing. And the significant level of interest is not confined to Denmark, but is growing everywhere.

In recent years, there has been a lot of hype surrounding 3D printing, but that is beginning to fade, says David Bue Pedersen, who holds Denmark's first PhD in 3D printing and Additive Manufacturing, and who is a postdoc at DTU Mechanical Engineering:

"People are finally coming to terms with what 3D printing can actually be used for. Several years ago, the mass media was pre-

dicting that 3D printing would replace all forms of production, which couldn't have been more wrong. 3D printing is just one technology out of many whereby companies can work with Additive manufacturing."

Additive manufacturing opens up three particularly interesting possibilities for companies: faster and less cost-intensive product development, products tailored to the individual customer (also called customizing), and local production.

Pedersen has just completed a three-year research project where, together with a large Danish enterprise, he has been testing 3D printing technology as an innovation tool at the company.

"We have been working with 3D printing to make the injection moulding of plastic more flexible. This will enable the company to develop new products faster and more cheaply," says Pedersen.



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# Transitioning From FR-4 to High-Frequency Materials

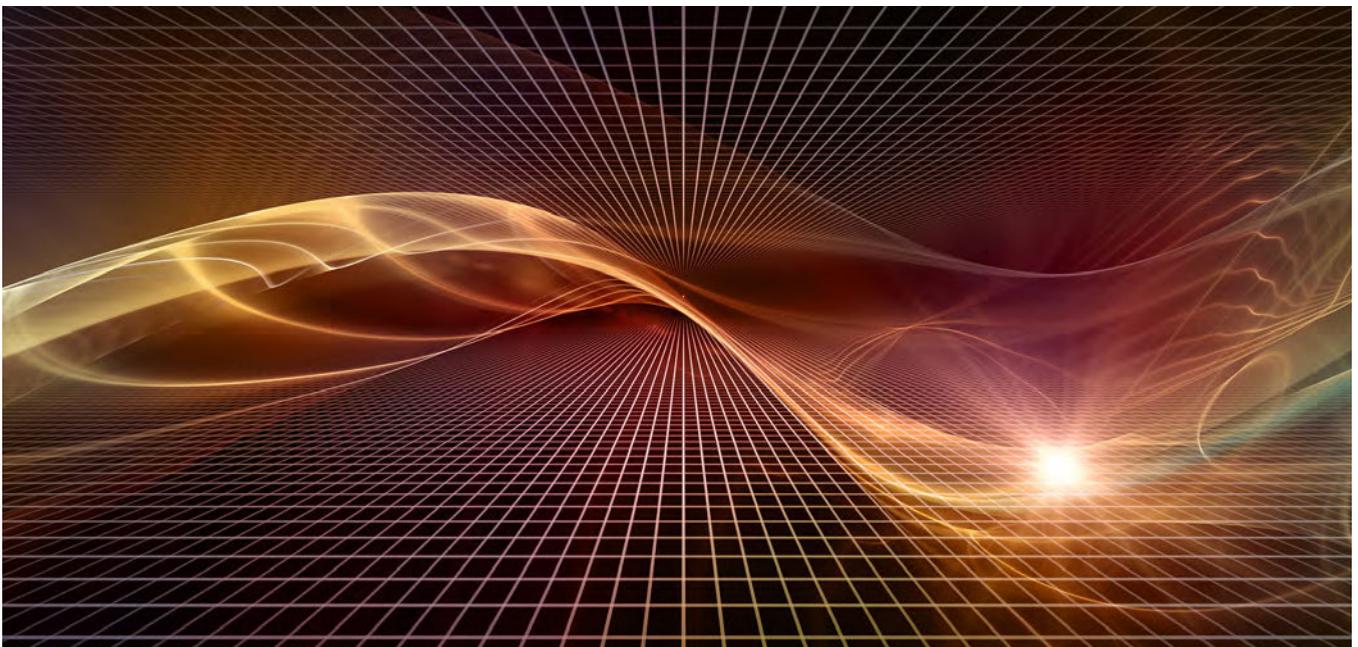
by **John Coonrod**  
ROGERS CORPORATION

The question of when to transition from FR-4 material to a higher performing material is typically not as straightforward as one may assume. Also, when the transition is obvious, a lot of unexpected issues may need to be addressed. Some of these issues can be related to the circuit design and others are related to the PCB fabrication process.

The move from FR-4 to a high-frequency material is often necessitated by the loss performance of a circuit. The acceptable amount of insertion loss for a particular circuit can vary greatly from one application to another. The material's loss is categorized by dissipation factor (Df) and it is rather subjective for what is considered low-loss, mid-loss and high-loss material. From my experience, I would categorize materials by Df as the following: high-loss material has a Df of 0.015 or greater and that is a pretty common value for many FR-4 materials. There are some high-performance FR-4 materials which have better loss, and some of these

have Df value of 0.010. I would consider these materials to be categorized mid-loss materials. Low-loss materials typically have Df values of 0.004 or less and extremely low-loss materials have a Df of 0.002 or less. There is a grey area between low-loss and mid-loss material where the range of Df is from about 0.004 to 0.010.

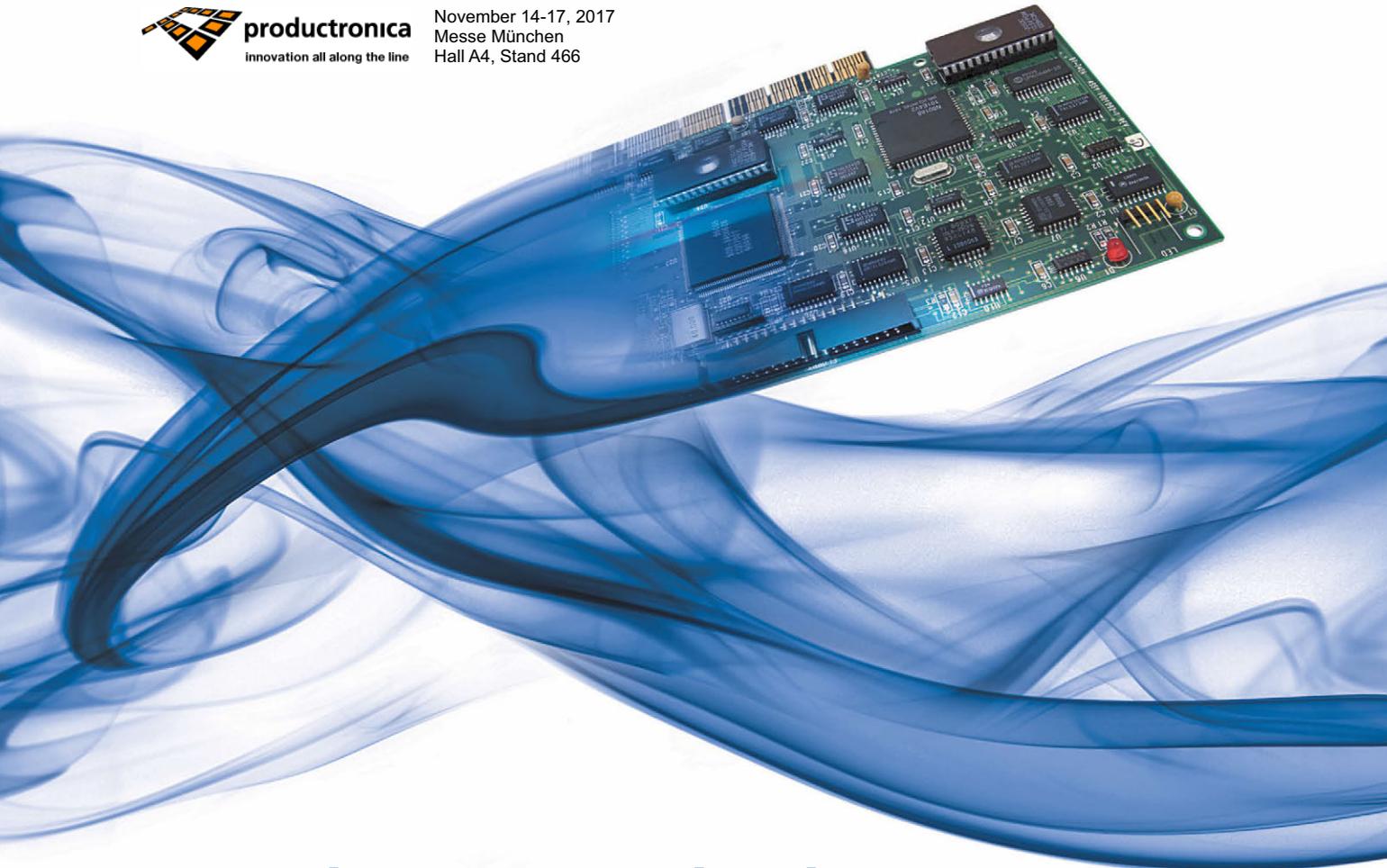
Besides the differences in loss, significant design changes may be necessary when switching to high-frequency materials. These changes are mostly due to FR-4 materials having a dielectric constant (Dk) value of about 4.2 to 4.5, while many high-frequency laminates have considerably lower Dk values. The change in Dk can cause impedance differences, so design changes to the conductor routing are often necessary. Additionally, the high-frequency laminate may not have the same substrate thickness offerings as the FR-4 materials and the thickness difference can require design changes in order to maintain the desired impedance and other critical electrical properties.





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Another issue is related to PCB fabrication processing. Some high-frequency materials are PTFE-based, and those type of materials can require very different processing parameters as compared to FR-4 materials.

There are other motivating factors for progressing on from FR-4. Due to the demands of the high-frequency industry, most high-frequency materials are formulated to have tighter Dk tolerance than FR-4 as well as offering tighter thickness control of the substrate. These tightly controlled laminate properties can be very beneficial for building a controlled impedance board with a narrow specification for impedance. Additionally, high-frequency materials are typically formulated to have very low moisture absorption and for certain applications that property may be more important than the benefit of the materials' lower Df. Lastly, high-frequency materials are typically formulated to have low thermal coefficient of Dk (TCDk), and this property is a measure of how much the Dk will change with a change in temperature. For certain applications, TCDk can be more critical than loss and this is another reason for using a high-frequency laminate.

Fortunately, new PCB materials are constantly being developed, and many of these bridge the gap between FR-4 and high-frequency materials. For instance, Rogers Kappa 438 has many attributes which are similar to FR-4, while offering many benefits associated with high-frequency materials. This material has a Df

value of 0.005; it is not as low as the Df of true low-loss materials, but it is obviously a significant improvement in loss as compared to the mid-loss or high-loss FR-4 materials.

The loss benefit can be important. However, Kappa 438 has been formulated to have the same Dk as many commonly used FR-4 materials. The Dk for this material is 4.38 and that means it can be used without significant modification to the circuit design, when replacing FR-4. Additionally, the Dk tolerance is much tighter than most FR-4 materials, at  $\pm 0.05$ . The moisture absorption is low, TCDk is low, and CTE is in a range where it can be used for high layer count PCB constructions and it can use the same processes as FR-4.

Of course, when changing to any different material for a PCB construction, it is recommended that the PCB fabricator optimize the process for the material in each particular build. But the good news is that, if you must make the transition from FR-4 to a high-frequency, low-loss material, there is a variety of available materials for the technologist to choose from.

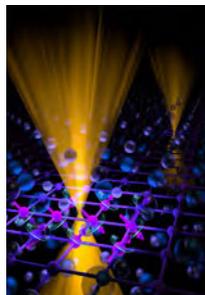
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**John Coonrod** is the technical marketing manager at Rogers Corporation.

## Scientists Discover New Magnet with Nearly Massless Charge Carriers

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terials” refers to materials where the current carrying electrons act as if they have no mass similar to the properties of photons, the particles that make up light. Amazingly, these electronic states are robust and immune to defects and disorder because they are protected from scattering by symmetry.

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- Perform defect reduction analysis and activities
- Participate in technology roadmap planning
- Participate in new materials, processing or other developments as required

### Experience & Education:

- BS degree in Engineering
- 2-5 years of proven work experience
- Excellent technical skills

Competitive salaries based on experience, comprehensive health benefits package, 401(k) and Quarterly Gain Sharing bonus available to eligible employees.

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## TECHNICA, U.S.A.

Fulfilling Manufacturing Needs  
Throughout the Electronics Industry

### Southern California Territory Sales Engineer

Technica, USA, a Western regional manufacturer's representative/distributor, has an open sales position for our Southern California territory. The position will be responsible for selling and servicing our entire product line within the specified territory to the PCB manufacturing industry.

This position requires a highly self-motivated, hands on, confident individual of the highest integrity.

#### Required Skills:

- BA/BS degree-desired, in a technical area is preferred
- Two years of outside/inside sales or manufacturing experience in the PCB manufacturing environment is desired
- Self-motivated self-starter with the ability to initiate and drive business with little supervision
- Independent worker with a strong commitment to customer satisfaction
- Understanding of consumable sales process
- Ability to organize activities and handle multiple projects simultaneously with effective and timely follow-up
- Ability to solve problems and make decisions for which there are no precedents or guidelines and be resourceful in nature
- Positive attitude while operating under pressure and be an independent problem-solver
- Computer skills in Windows, Outlook, Excel, Word and PowerPoint
- Must have a valid driver's license with good driving record

Please send resume.

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## TECHNICA, U.S.A.

Fulfilling Manufacturing Needs  
Throughout the Electronics Industry

### Western Regional Equipment Service Technician

Technica, USA, a Western regional manufacturer's representative/distributor has an opening for an equipment service technician covering the Western USA, including but not limited to, California, Oregon, Washington, Utah, Colorado, and Arizona. The position will be responsible for servicing our PCB fabrication equipment product line, including installation, troubleshooting, repair service, rebuild service, etc. This position requires a highly self-motivated, hands on, confident individual of the highest integrity.

Key responsibilities are to install and service equipment, conduct equipment audit, and provide technical service when appropriate to solve problems.

#### Required Skills:

- 2+ years of experience in a PCB manufacturing environment or similar
- Willing to travel
- Positive "whatever it takes" attitude while operating under pressure
- Self-motivated self-starter with the ability to initiate action plans
- Ability to work independently with a strong commitment to customer satisfaction
- Excellent communication and interpersonal skills
- Strong ability to use all resources available to find solutions
- Computer skills with ability to write detailed service and equipment reports in Word
- Understanding of electrical schematics
- Able to work in and around equipment, chemical, and environmental conditions within a PCB manufacturing facility

Please send resume.

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# CAREER OPPORTUNITIES



**LENTHOR ENGINEERING**  
MAKING THINGS FLEXIBLE IN A RIGID WORLD®  
311 Turquoise Street Milpitas, CA 95035 (Phone) 408-945-8787

## SALES ACCOUNT MANAGER

This is a direct sales position responsible for creating and growing a base of customers. The account manager is in charge of finding and qualifying customers while promoting Lenthor's capabilities to the customer through telephone calls, customer visits and use of electronic communications. Experience with military and medical PWB/PWA a definite plus. Each account manager is responsible for meeting a dollar level of sales per month and is compensated with salary and a sales commission plan.

### Duties include:

- Marketing research to identify target customers
- Initial customer contact (cold calling)
- Identifying the person(s) responsible for purchasing flexible circuits
- Exploring the customer's needs that fit our capabilities in terms of:
  - Market and product
  - Circuit types used
  - Quantity and delivery requirements
  - Competitive influences
  - Philosophies and finance
  - Quoting and closing orders
  - Bonding
- Submitting quotes and sales orders
- Providing ongoing service to the customer
- Problem solving
- Developing customer information profiles
- Developing long-term customer strategies to increase business
- Participate in quality/production meetings
- Assist in customer quality surveys
- Knowledgeably respond to non-routine or critical conditions and situations

Competitive salaries based on experience, comprehensive health benefits package and 401(k) Plan.

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## Experienced PCB Sales Professional

With more than 30 years of experience, Prototron Circuits is an industry leader in the fabrication of high-technology, quick-turn printed circuits boards. Prototron of Redmond, Washington, and Tucson, Arizona are looking for an experienced sales professional to handle their upper Midwest Region. This is a direct position replacing the current salesperson who is retiring after spending ten years with the company establishing this territory.

The right person will be responsible for all sales efforts in this territory including prospecting, lead generation, acquiring new customers, retention, and growth of current customers.

This is an excellent opportunity for the right candidate. Very competitive compensation and benefits package available.

For more information, please contact Russ Adams at 425-823-7000, or [email your resume](#).

apply now

## Process Engineer (Redmond, Washington)

With more than 30 years of experience, Prototron Circuits is an industry leader in the fabrication of high-technology, quick-turn printed circuits boards. We are looking for an experienced PCB process engineer to join the team in our Redmond, Washington facility. Our current customer base is made up of forward-thinking companies that are making products that will change the world, and we need the right person to help us make a difference and bring these products to life. If you are passionate about technology and the future and believe you have the skills to fulfill this position, please contact Kirk Williams at 425-823-7000 or [email your resume](#).

apply now



Arlon EMD, located in Rancho Cucamonga, California is currently interviewing candidates for **manufacturing and management positions**. All interested candidates should contact Arlon's HR department at 909-987-9533 or fax resumes to 866-812-5847.

Arlon is a major manufacturer of specialty high performance laminate and prepreg materials for use in a wide variety of PCB (printed circuit board) applications. Arlon specializes in thermoset resin technology including polyimide, high Tg multifunctional epoxy, and low loss thermoset laminate and prepreg systems. These resin systems are available on a variety of substrates, including woven glass and non-woven aramid. Typical applications for these materials include advanced commercial and military electronics such as avionics, semiconductor testing, heat sink bonding, high density interconnect (HDI) and microvia PCBs (i.e., in mobile communication products).

Our facility employs state of the art production equipment engineered to provide cost-effective and flexible manufacturing capacity allowing us to respond quickly to customer requirements while meeting the most stringent quality and tolerance demands. Our manufacturing site is ISO 9001:2008 registered, and through rigorous quality control practices and commitment to continual improvement, we are dedicated to meeting and exceeding our customer's requirements.

[more details](#)



## PCB Process Planner

Accurate Circuit Engineering (ACE) is an ISO 9001:2000 certified manufacturer of high-quality PCB prototypes and low-volume production for companies who demand the highest quality in the shortest time possible. ACE is seeking a skilled individual to join our team as a PCB process planner.

### Responsibilities will include:

- Planning job travelers based on job release, customer purchasing order, drawings and data files and file upon completion
- Contacting customer for any discrepancies found in data during planning and CAM stage
- Consulting with director of engineering regarding technical difficulties raised by particular jobs
- Informing production manager of special material requirements and quick-turn scheduling
- Generating job material requirement slip and verify with shear clerk materials availability
- Maintaining and updating customer revisions of specifications, drawings, etc.
- Acting as point of contact for customer technical inquiries

Candidate should have knowledge of PCB specifications and fabrication techniques. They should also possess good communication and interpersonal skills for interfacing with customers. Math and technical skills are a must as well as the ability to use office equipment including computers, printers, scanners, etc.

This position requires 3 years of experience in PCB planning and a high school level or higher education.

[apply now](#)

# TOP TEN



## Recent Highlights from PCBDesign007

### 1 Using Vibration and Acceleration Analysis to Improve Reliability

In harsh environments, fatigue can be responsible for up to 20% of failures. Customers have come to expect reliability across the industry spectrum no matter where actual production occurs. Reliable products have less risk of failure, less field returns and less warranty claims, all of which contribute to higher profitability.



### 3 Beyond Design: FPGA PCB Design Challenges

The primary issue is generating optimal FPGA pin assignments that do not add vias and signal layers to a PCB stackup or increase the time required to integrate the FPGA with the PCB. Engineers generally do not consider FPGA pin assignments that expedite the PCB layout. Hundreds of logical signals need to be mapped to the physical pin-out of the device, and they must also harmonize with the routing requirement.



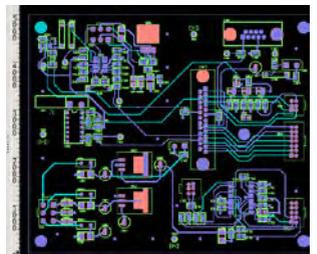
### 2 Ultra Librarian Gets Advanced PDF Scraping Capabilities from Existing EMA Tech

"This is the first collaborative development effort for the Ultra Librarian desktop software since EMA acquired Accelerated Designs," said Manny Marcano, president and CEO of EMA. "This allowed us to very quickly enhance the software to give our customers faster part creation and higher fidelity output with a significant reduction in download size."



### 4 Ucamco Provides Free Reference File Viewer for Gerber Users

Ucamco is now offering a free Gerber reference file viewer for the Gerber user community. The viewer provides an easy way to see the correct interpretation of a file. Diagnostics tools help to analyze it. If the viewer reverse-engineers an image on an invalid file, it will give a warning that the file contains errors, thus helping to detect invalid files.



## 5 PCB Designers Notebook: Embedding Components, Part 2

Technology and processes for embedding capacitor and inductor elements rely on several unique methodologies. Regarding providing capacitor functions, IPC-4821 defines two methodologies for forming capacitor elements within the PCB structure: laminate-based (copper-dielectric-copper) or planar process and non-laminate process using deposited dielectric materials.



## 6 Cadence Reports Revenue of \$479 Million in Q2 2017

Cadence reported second quarter 2017 revenue of \$479 million, compared to revenue of \$453 million reported for the same period in 2016. On a GAAP basis, Cadence recognized net income of \$69 million in the second quarter of 2017, compared to net income of \$49 million for the same period in 2016.



## 7 Embedded Technology: A Useful Tool in Freedom CAD's Toolbox

Freedom CAD has been designing and fabricating boards with embedded technology for years, and doing some innovative work along the way. I asked Scott McCurdy, Freedom CAD's director of sales and marketing, to share some details about their embedded processes, as well as the challenges and opportunities that embedded technology offers.



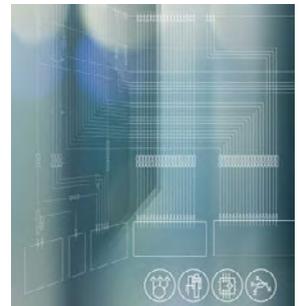
## 8 CircuitData: A New Open Standard for PCB Fab Data Exchange

Widely reported recently has been the development of a new open standard for exchanging printed circuit fabrication data by an independent international task group with members from the entire supply chain. Initiated by Norway-based Elmatica, the CircuitData standard is designed to enhance your Gerber, ODB++ and IPC-2581 files, and not replace them.



## 9 Zuken Launches E3.series 2017

The latest release contains new and enhanced functionality that further increases productivity throughout all phases of engineering, from design to manufacture. New third-party integrations extend the E3.series ecosystem of solutions.



## 10 Artificial Machines Standardizes on Mentor EDA Solutions to Develop Smart Machine IP

The smart machine design company Artificial Machines has standardized on Mentor EDA solutions. The competitive replacement includes leading-edge Mentor solutions such as Xpedition printed circuit board (PCB) design, Hyperlynx simulation, Valor manufacturing validation and ASIC chip design tools.



***PCBDesign007.com for the latest circuit design news and information—anywhere, anytime.***

# Events



For IPC Calendar of Events,  
[click here](#).

For the SMTA Calendar of Events,  
[click here](#).

For a complete listing, check out  
The PCB Design Magazine's  
[event calendar](#).

## [NEPCON South China 2017](#)

August 29–31, 2017  
Shenzhen, China

## [PCB West](#)

September 12–14, 2017  
Santa Clara, California, USA

## [24<sup>th</sup> FED Conference](#)

September 15–16, 2017  
Bonn, Germany

## [SMTA International 2017 Conference and Exhibition](#)

(IPC Fall Committee meetings held in conjunction with SMTAI)  
September 17–21, 2017  
Rosemont, Illinois, USA

## [IPC Fall Standards Development Meetings](#)

September 16–21, 2017  
Rosemont, Illinois, USA

## [electronicAsia](#)

October 13–16, 2017  
Hong Kong

## [IPC Flexible Circuits: HDI Forum](#)

October 17–19, 2017  
Minneapolis, Minnesota, USA

## [TPCA Show 2017](#)

October 25–27, 2017  
Taipei, Taiwan

## [productronica 2017](#)

(IPC Committee meetings held in conjunction with productronica)  
November 14–17, 2017  
Munich, Germany

## [HKPCA/IPC International Printed Circuit & South China Fair](#)

December 6–8, 2017  
Shenzhen, China

## [47<sup>th</sup> NEPCON JAPAN](#)

January 17–19, 2018  
Tokyo Big Sight, Japan

## [DesignCon 2017](#)

January 30–February 1, 2018  
Santa Clara, California, USA

## [EIPC 2018 Winter Conference](#)

February 1–2, 2018  
Lyon, France

## [IPC APEX EXPO 2018 Conference and Exhibition](#)

February 27–March 1, 2018  
San Diego, California, USA

## [KPCA Show 2018](#)

April 24–26, 2018  
Kintex, South Korea

## [Medical Electronics Symposium 2018](#)

May 16–18, 2018  
Dallas, Texas, USA

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