I-Connect007

APRIL 2019

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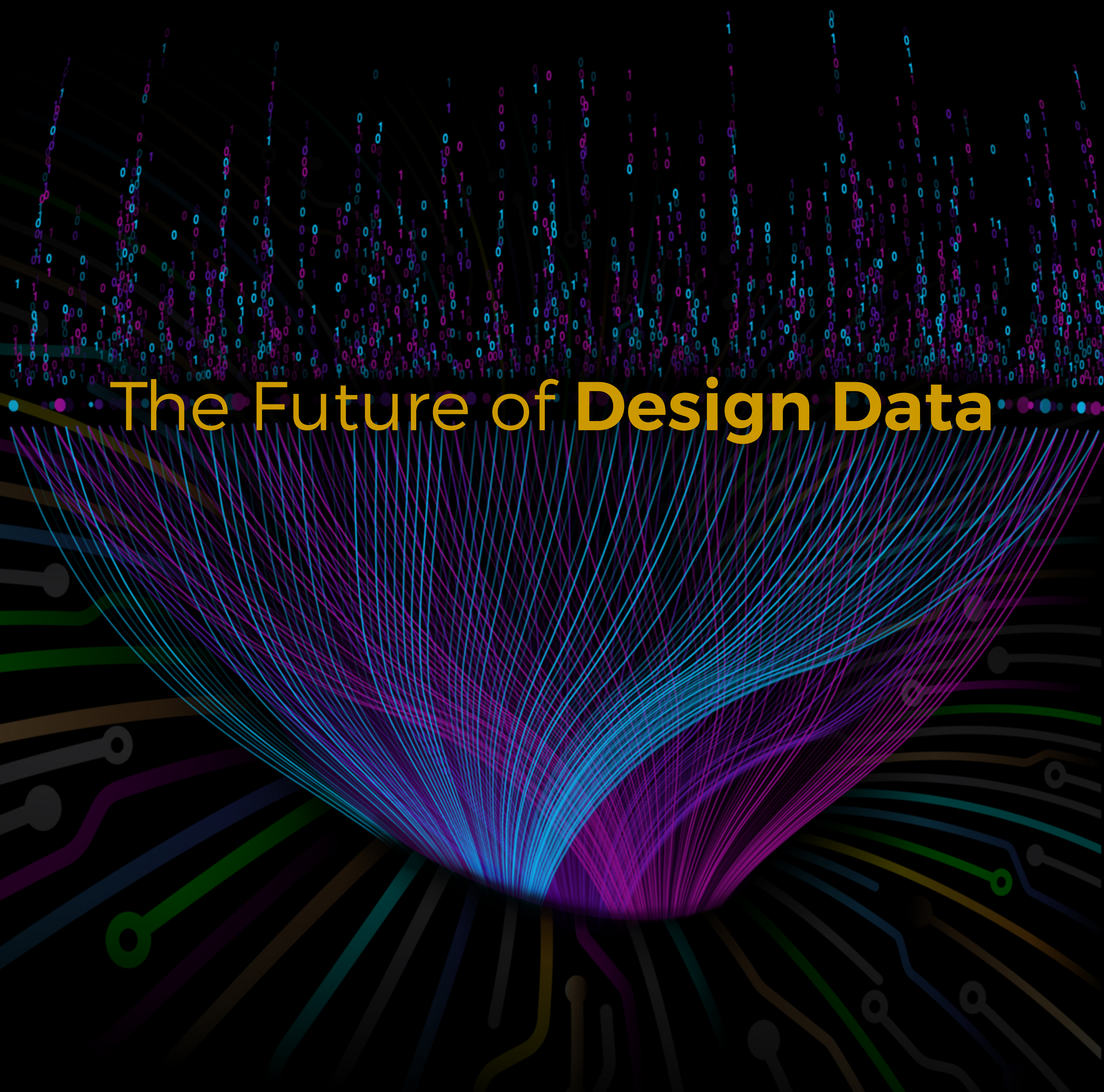

The Future of **Design Data**

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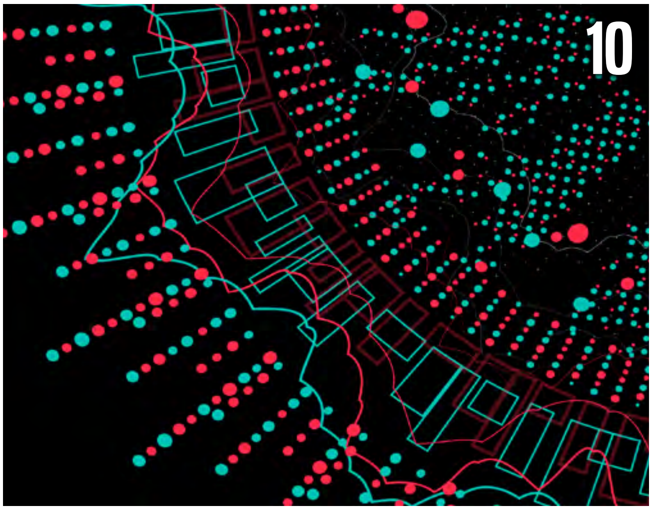
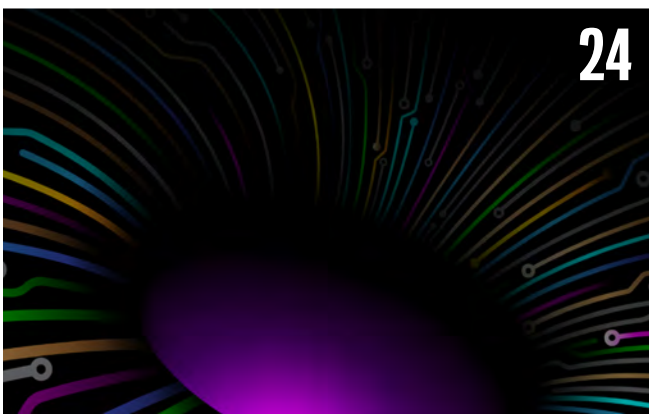


The Future of Design Data

We've all heard quite a bit of chatter about smart manufacturing over the past few years. Everyone involved in designing, fabricating and assembling PCBs wants to get on board. But what does this mean for CAD data? What do designers need to do differently to take full advantage of smart technologies such as Industry 4.0 and IPC's Connected Factory Exchange (CFX)?



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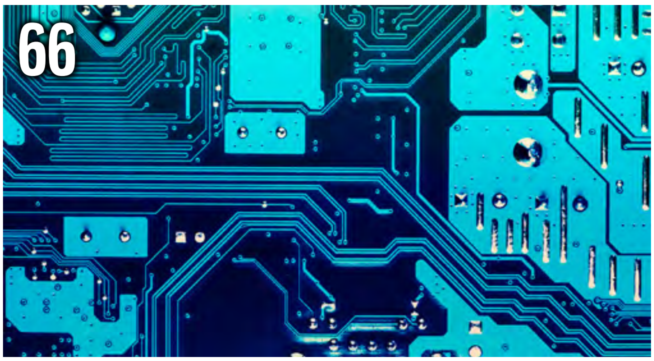

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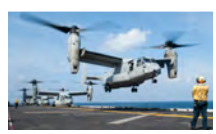


Get Smart!

The Shaughnessy Report

by Andy Shaughnessy, I-CONNECT007

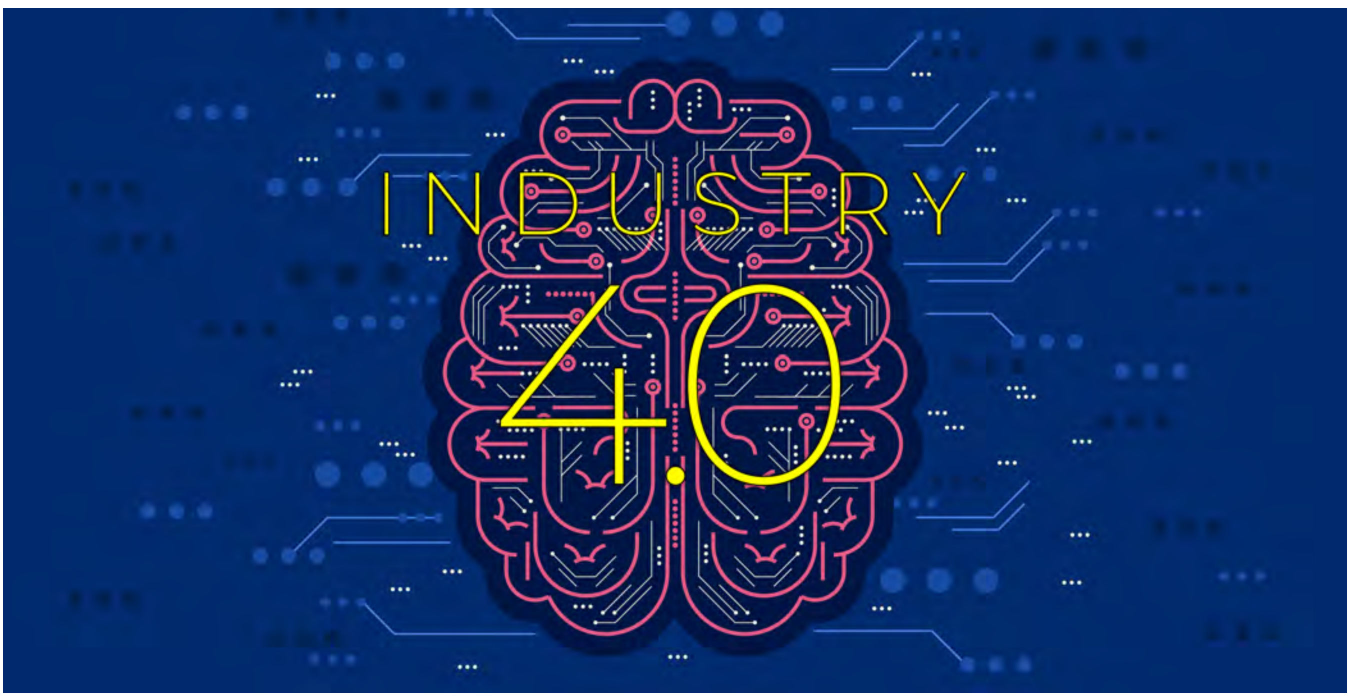
It sounds so perfect—"smart" manufacturing. That must be what we've needed all along! We've had enough of this "average intelligence" manufacturing. Yes, we've heard quite a bit of chatter about smart manufacturing over the past few years. Whatever "smart" means to you, everyone involved in designing, fabricating, and assembling PCBs wants to get on board.

The PCB community in the U.S. often feels like it's a little behind the curve compared to other industries, and that's definitely the case here. Manufacturers in Asia have already seen gains in efficiency, productivity, and sustainability by adopting integrated, collaborative, data-driven processes. The North American PCB fabrication community is playing catch-up regarding smart manufacturing and Industry 4.0.

At the same time, many U.S. PCB designers are curious about what this smart new world means to them and their "old-school" CAD data. Fabricators in the states can also be forgiven for wondering the same thing, especially when CAM departments receive so many inaccurate or incomplete design data packages. Is PCB design ready for smart manufacturing? What are designers going to have to do differently for OEMs to take full advantage of smart technologies, such as Industry 4.0 and IPC's Connected Factory Exchange (CFX)?

We asked some of our expert contributors to share their thoughts and opinions about smart manufacturing and what this means for the PCB designers and design engineers on the front end.

Our first feature is by Patrick McGoff, market development manager, and David Wiens, Xpedition product marketing manager, both with Mentor, a Siemens business. They explain how intelligent design data is a necessity for smart processes, and why the information in a simple bill of materials (BOM) will not be adequate for manufacturing in the future.



Next, columnist Michael Ford, senior director of emerging industry strategy for Aegis Software, discusses some of the challenges ahead for smart design and manufacturing, including the need to embrace "adaptive" planning, which may be best achieved by utilizing a combination of formats, such as IPC-2581 for design data and CFX for manufacturing.

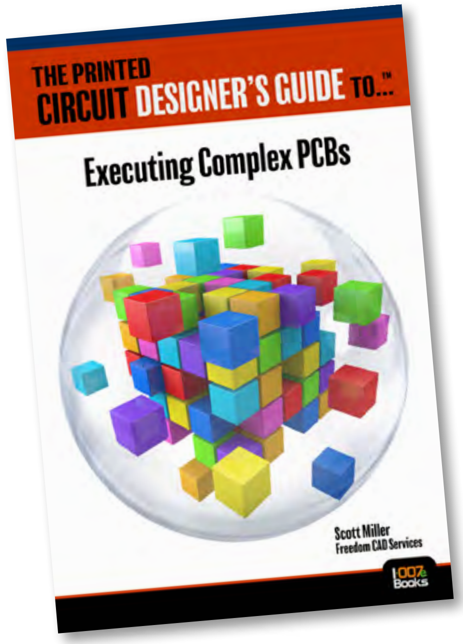
Then, we have a short feature by Technical Editor Happy Holden who offers some background on computer-integrated manufacturing and investigates the way CAD data fits into the equation.

Switching gears, Denis Morin, Karel Tavernier, Jean-Pierre Charras, and Marius Matioc of Ucamco take the reader through the new XNC format—a collaboration by Ucamco, KiCad, and PentaLogix—which updates the Gerber drill data transfer process. We also have an interview with Robert Huxel, XPLM's director of business development, who outlines the company's PLM software and XPLM's role in integrating ECAD and MCAD data and explains why this convergence is so important for the future of PCB design.

Next, we feature a great article by Keysight Technologies' Chang Fei Yee who focuses on the impact of copper pour on insertion loss and impedance. We also bring you columns by our regular contributors, including Stephen V. Chavez of the IPC Designers Council, Bob Tise of Sunstone Circuits, Alistair Little of Electrolube, Barry Olney of iCD, and John Coonrod of Rogers Corporation.

Thus far, the facts point to smart manufacturing being the way forward for PCB design and manufacturing. By relying on adaptive planning instead of the old long-term way, companies should be able to make quick, data-driven decisions that cut costs and drive up productivity. But the hoopla also reminds me of the early days of Lean. Everyone wanted to say that their company was Lean, but many companies wound up paying a Lean expert six figures to show them how to implement a plan that they never used. Have company owners learned from that experience?

Being late to the party isn't usually a good thing, but the success that smart manufacturers have seen in Asia might actually help sway the "mature" technologists on our shores into adopting smart manufacturing.



Freedom CAD's eBook Now Available

If you design sophisticated circuit boards for a living, you're in luck. Our friends at Freedom CAD have just written a new I-Connect007 eBook, *The Printed Circuit Designer's Guide to… Executing Complex PCBs*.

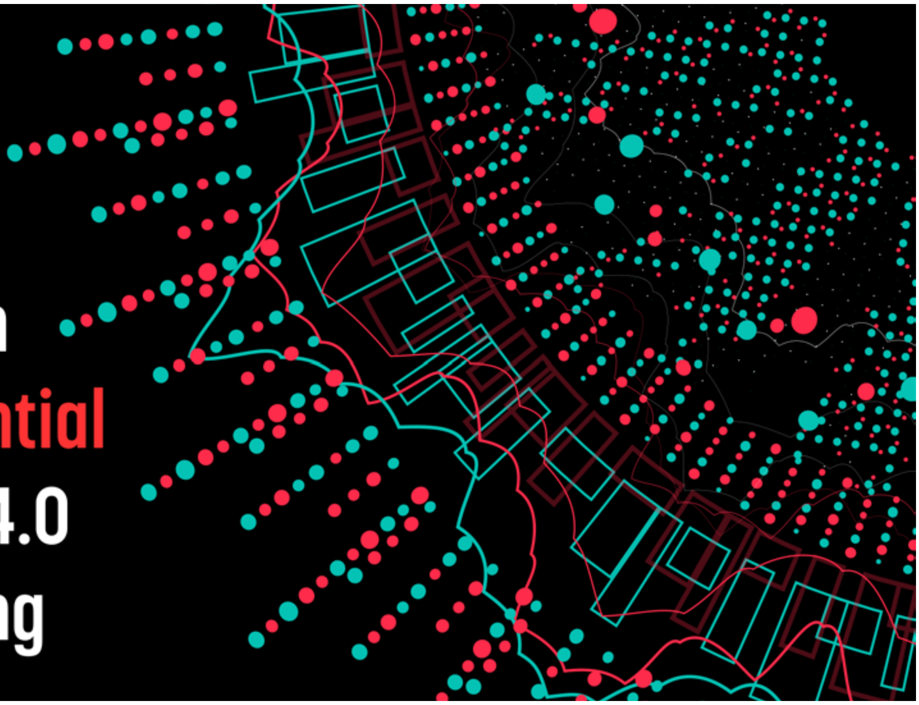
Freedom CAD's Scott Miller provides a set of guidelines for designing the most complex, high-speed circuit boards. He and his veteran PCB design team share real-world examples that can help designers like you, from the planning stages and schematic capture through documentation and successful data handoff.

It's also an entertaining book to read. Sure, I may be a little bit biased because I helped edit it, but check it out for yourself. It's free to download; just click here.

And if you're not already a subscriber to *Design007 Magazine,* what are you waiting for? Subscribe here. See you next month! **DESIGN007**

Andy Shaughnessy is managing editor of *Design007 Magazine.* He has been covering PCB design for 19 years. He can be reached by clicking here.

Smart Design Data Is Essential for Industry 4.0 Manufacturing



Feature by Patrick McGoff and David Wiens
MENTOR, A SIEMENS BUSINESS

Almost all of the conversation regarding Industry 4.0 is centered on the manufacturing floor, which is where the effect of the initiative is most felt initially. Little attention is given to the starting data for manufacturing—the data that comes from design. However, you can't have smart manufacturing if your process begins with dumb data. As Pink Floyd said, "You can't have your pudding if you don't eat your meat!"

Industry 4.0 starts with smart data. Smart data means a complete dataset with intelligence embedded within it. Wikipedia defines Industry 4.0 as "a name given to the current trend of automation and data exchange in manufacturing technologies." Data exchange is a pillar of Industry 4.0.

If the data can't be computed, exchanged, and interpreted automatically, inputs must be interpreted by humans to determine how to process the job. Smart data allows automated processing from design for manufacturing (DFM) and design for test (DFT) to stencil generation, surface-mount technology (SMT), and test programming. It's as simple as an if/then statement: if this condition exists, then take that action. If the system doesn't know what this data represents, then it can't do anything with it automatically.

Digitalization of the PCB manufacturing product model is smart data. It defines the PCB to be manufactured; and in so doing, it also defines the manufacturing processes required (Figure 1). The PCB design process evolves the

System Definitions	Design and Simulation	Manufacture
Requirements, Configurations & System Modeling	Mechanical Design & Verification	Mechanical Manufacturing
	Electronic Design & Verification	PCB Manufacturing
	EDS, Network & Harness Design	Harness Manufacturing
	Software Engineering & Verification	Software Production

Figure 1: Smart data enables seamless collaboration from product requirements through manufacturing, across multiple domains.

digital product model from concept to manufacturing hand-off with a lot of multidiscipline collaboration required along the way (such as schematic/layout, ECAD/MCAD, harness/board, system/boards). Each step requires smart data to collaborate, and many checks along the way to ensure that nothing is corrupted during the collaboration process.

At the PCB design stage, the major elements include:

- Component information (e.g., footprint, pin contact areas, pin numbers, 3D geometry, package type, part number, simulation models, cost, status, compliance, etc.)
- Schematics
- Multiboard structure
- 3D board (e.g., metal traces and shapes; net properties; HDI, blind, buried, and/or through vias; materials stackup; rigid-flex regions; etc.)
- System connectivity
- Constraint sets for performance, mechanical structure, and manufacturability

Back in the origins of CAD, designs were much less intelligent (designers were just happy it wasn't tape). But over time, attributes have been added so that a design isn't just 2D geometries; it's filled with "smarts," such as net names and types, rule sets, impedances, materials, manufacturers, region types, and package constructs. Unfortunately, often, all of this intelligence is stripped away when the data is sent to manufacturing, burdening them to recreate the intelligence to effectively tool the job.

The PCB manufacturing industry speaks of the goal to build a lot size of one. The trend in electronics is certainly in the direction of smaller lot sizes but think about the manufacturing front-end engineering responsibilities today. They must take in a multitude of design data files, each of various formats and frequently with incomplete or conflicting data. Because the majority does not contain intelligent attributes or properties, a manufacturing engineer is tasked with reverse engineering the data so that the proper work instructions, tooling, and programming can be done.

Whenever the data package is incomplete or contains contradicting data, the job is put on hold while it is resolved with the customer. Optimizing for a lot size of one is impossible if your front-end engineering consumes days of manual effort. Contrast that with Amazon. Do you think they could be proficient fulfilling your order of a lot size of one without automation? Optimization equates to efficiency—it's a low-cost producer without sacrificing quality.

An excellent paper by Roland Berger, "Industry 4.0 and Its Impact on Electronics Assembly," defines 20 building blocks of Industry 4.0, and one of them is DFM. At a basic level, this is the process of determining if the PCB design can be manufactured without issue, or ideally, whether the PCB design has been optimized for manufacturing—that is, it can be manufactured and tested at the lowest possible cost with the highest yield and reliability. If the PCB design data input to the DFM software has the full set of attributes and properties as exists in the electronic design automation (EDA) data, then the DFM software can automatically identify which DFM checks are applicable for that design and what is the correct technology classification to use in selecting the right DFM rules values.

For instance, if the design data is represented in ODB++ format, the receiving DFM system will know the construction is sequential lamination and which layers each of the drill files span. It can then perform DFM checks based on microvia and HDI technology without any human intervention. Without that level of intelligence, the DFM user would need to re-establish the layer construction and associated drill files to the appropriate layers before they then have to determine the DFM rule sets to use. You might say it's not rocket science, but what happens when the drill drawing contradicts the layer names in the data files? Smart data eliminates that potential risk and allows for a streamlined DFM process (Figure 2).

On the assembly side of DFM, we need to know component and lead types and IPC clas-

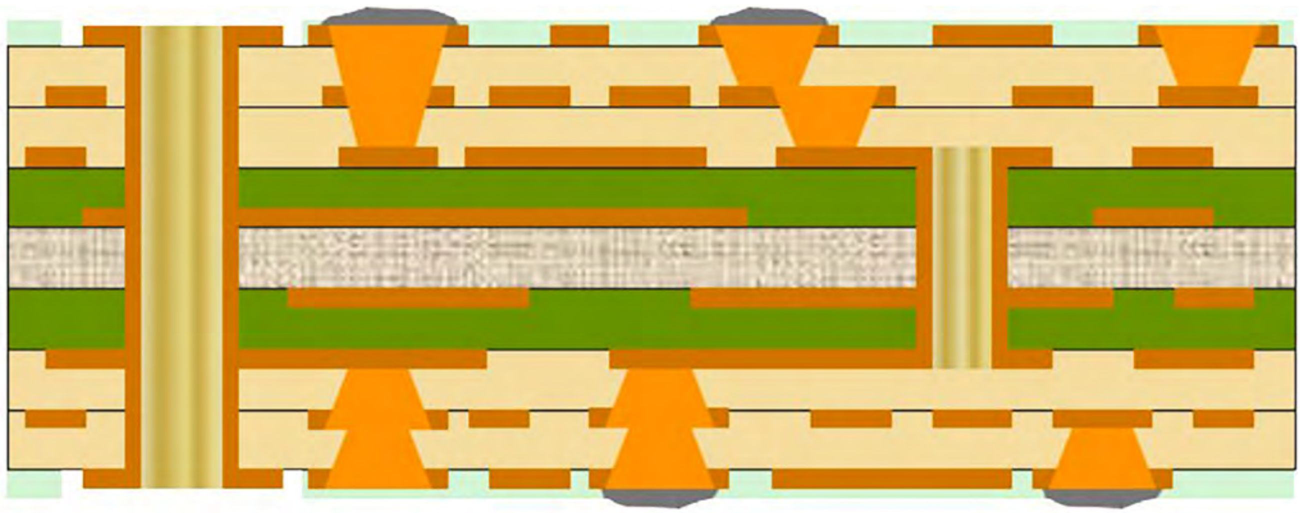


Figure 2: Intelligent data allows DFM software to automatically recognize an HDI design.

sifications. Merely having a bill of materials (BOM) doesn't tell us everything we need. The BOM doesn't give us an easy way to determine if we have a tall component too close to a routed slot. Nor can it tell us if the AOI system is going to have difficulty seeing adjacent leads because of shadowing from tall components. But when the BOM is merged with the CAD data to make intelligent data, all of the necessary manufacturing checks can be automated.

Product testability is another critical element of the deliverable to manufacturing. If the product is not easily testable, the ability to deliver cost-effective functioning boards is affected. In the same way, good DFM principals are now part of the design process, good DFT is needed throughout the process. Leaving it to the end, or not addressing it at all, delivers an incomplete product model to manufacturing, which affects deliveries, quality, and overall product cost.

The requirement for smart data is not limited to conventional rigid PCBs. Smart data is required for flex and rigid-flex technologies because they use different materials and design features. The DFM system must be able to know automatically where the bend area is as well as the stiffener, coverlay, and silver mask zones (Figure 3).

We also need to think of smart data in terms of digitally modeling the manufacturing processes. This digital twin of manufacturing processes enables designers to benefit from intelligent DFM concurrent with the layout process—the left-shift strategy. If designers can identify areas to improve their PCB design while they are doing the design, they greatly reduce the number of revisions necessary to ramp their designs to volume production. The digital manufacturing twin of process capabilities makes it easier for them to achieve this optimization without having to possess the

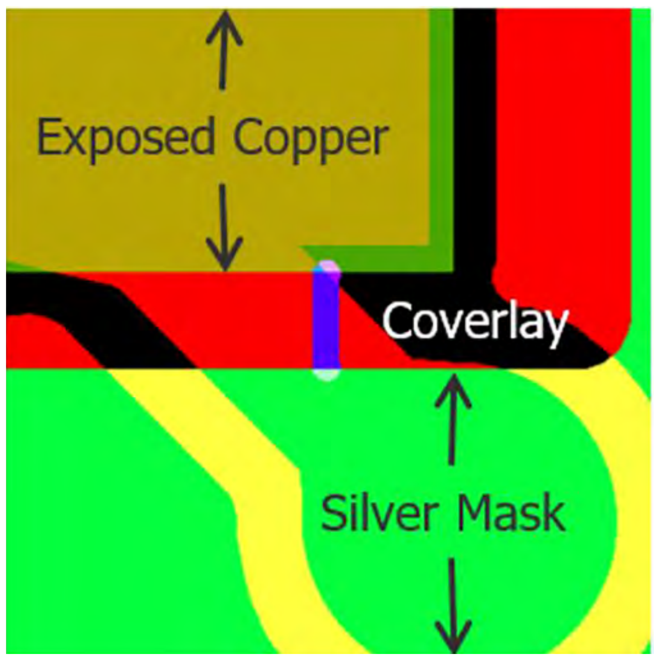


Figure 3: Proper DFM of flex circuits requires intelligent data from EDA to systematically identify the various zones of material.

manufacturing expertise because it's built into the system.

However, the manufacturing digital twin is not limited to a single supply partner. Ideally, you would have a digital twin of all of your manufacturing partners' capabilities so that you could see an aggregate impact of your designs.

Material optimization is another element of the digital twin. Being able to see the material utilization of the assembly panel design based on your fabricator's panel sizes gives you the ability to adjust the assembly panel configuration to lower your costs. A rotation of a board or a nesting of boards may permit you to get additional boards on every panel, and that equates to savings for you.

All of this aligns with the objectives of Industry 4.0. In probably the best summary statement of Industry 4.0 that I have seen, Daniela Schäffer of Murrelektronik GmbH [1] states, "Digitization is becoming a great opportunity for many companies. The challenge will be to digitize the right thing and use Industry 4.0 not only as a 'showcase object' but also as an instrument for optimization."

In the future, we can expect advances in automation of the feedback from manufacturing. Today, the DFM rules are updated manually based on the manufacturing lessons learned. Looking ahead, it makes sense that if the quality data has the same level of smarts as the DFM data, the DFM rules could be dynamically updated based on user-defined criteria.

Additionally, we can envision predictive analytics finally becoming mainstream. What if you could apply empirical manufacturing and quality data on a new design to predict yield, cost, and reliability based on the technology, materials, and manufacturing processes required? Unless the manufacturing data collected is applied with the same level of intelligence and automation back to design, Industry 4.0 will not reach its full potential.

Smart data empowers automation, which drives efficiencies, even at a lot size of one. That is the whole objective of Industry 4.0. Why start your smart manufacturing strategy with a handicap? Insist on smart data instead. **DESIGN007**

Reference

1. "German Industry 4.0 Index 2018," a study from Staufen AG and Staufen Digital Neonex GmbH.

Patrick McGoff is a market development manager for Mentor, a Siemens Business.

David Wiens is Xpedition product marketing manager with Mentor, a Siemens Business.

Tiny Silicon Nanoparticles Cement New Era for Ultra-high Capacity Batteries

Scientists believe that silicon could be the answer to your battery woes with the potential for a charge capacity 10 times larger than current lithium-ion batteries. But silicon has a tendency to fracture and break with numerous charge and discharge cycles due to volume expansion and contraction as silicon absorbs and releases lithium ions.

SiX-COOH/GA

Now, University of Alberta chemists have published research that takes a critical step in solving this problem, studying the effect of nanostructuring the silicon within lithium-ion batteries to understand the importance of size.

Researchers examined silicon nanoparticles of four different sizes within highly conductive graphene aerogels. The results show that the smaller the particle, the less likely it is to crack or fracture upon lithiation.

The next steps are to develop technology for creating silicon nanoparticles in a faster and less expensive way, making these tools more accessible for industry and technology developers. (Source: University of Alberta)

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The human body is an extremely complex "electrical (neurological) system", with companies continuing their quest to understand and improve capability as related to neural interface, basically connecting the human body directly into computers! There is no question, capabilities in smart phone/watch technologies connected to the internet erases any doubt of the potential to connect people to computers.

With the brain being the human equivalent of the "MicroProcessor", semiconductor companies such as IBM, Intel, MicroChip and MicroSemi have been well aware of potential for connectivity. Others have taken knowledge of neural interface to help humans manage their internal electrical systems, including Medtronic, Philips and Abbott, with a range of pacemakers, defibrillators and neural therapies.

Expanding the potential scope of linking the brain to computers and to the internet has attracted the likes of Amazon, Apple, Facebook, Google, MicroSoft, Neuralink and others, adding to the list that already includes J&J, G.E., T.I., Stryker, and Edwards. MicroProcessors and other ASIC Chips, coupled with MEMS and Sensors, are now seen as the "next-big-thing" over the next 5 years looking at the Internet-of-Things (IoT).

This event will bring together experts to cover topics such as:

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- MEMS, Sensors and Integrated Circuits
- Implantable Devices and Neural Interface
- Medical Robotics, Equipment, and Prosthetics
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Standards-driven, Digital Design Flow for Industry 4.0

Accelerating Tech—Insights from the Smarter Factory

Feature Column by Michael Ford, AEGIS SOFTWARE

The term "fragmented manufacturing" is a good way to describe current assembly manufacturing challenges in an Industry 4.0 environment. Even in Germany, productivity reportedly continues to decline. To reach the upside of Industry 4.0, data flows relating to design play a major role—one that brings significant opportunity to the overall assembly business.

The assembly sector always complains about the increasing mix of products that are being scheduled together with lower volumes. It's ironic when we consider the massive growth in the application of electronics into virtually every device that we use. Surely, that means that volumes overall should be going up.

Unfortunately, the industry has become like an old, mechanical hard disk. We are trying to squeeze through more and more data into a device that appears to be working more slowly, but the files on the disk have become fragmented. Instead of the data being stored in one long group record, files are split up into many pieces and stored in different places on the disk. It is as if instead of going to the supermarket, you have to pick up groceries from many shops on the high street, one by one. Windows 10 now turns on periodic hard-disk defragmentation automatically, so most people don't even notice this issue anymore. Can we do the same in our assembly manufacturing plants?

Assemblers have been driven to reduce or eliminate finished goods stock from the warehouse all the way through to the customer with direct shipping preferred over the investment of stock in an expansive distribution chain and risk of depreciation as market demands change. This is in part a great opportunity for the resurgence of local manufacturing and a key driver of Industry 4.0. The assembly schedule, therefore, has to meet the almost daily requirements of the customer, over the complete range of products made. Hence, the high-mix and low-volume scenario.

As this is a long-term significant business driver, assembly cannot continue to cling to the paradigm of optimized long-term planning as core parameters change every day. What is really needed is a way to manage the allocation of products to assembly line configurations immediately in a way that optimizes the utilization of resources. Accepting that we have to visit individual stores on the high street does not preclude us from planning to visit them in an efficient fashion, creating a sequenced journey that minimizes the walking distance from one to another.

As this is a long-term significant business driver, assembly cannot continue to cling to the paradigm of optimized long-term planning as core parameters change every day.

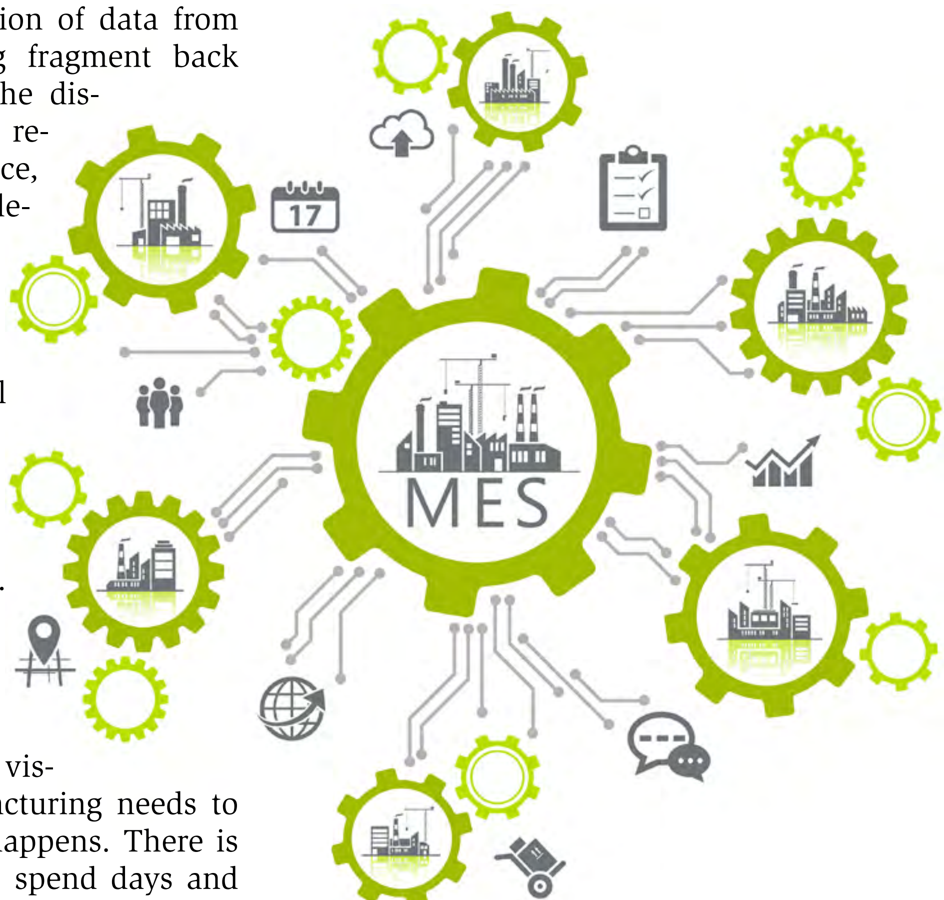
Having seen the evolution of the core business requirement, Aegis Software has been driving industry change through the use of new technology based on standards for some time. Assembly engineering and manufacturing are now going through a fundamental change to address the production fragmentation problem. Adaptive planning is a critical new solution within a modern digital engineering solution. The best practice flow is to receive the complete product design data inclusive of all required documentation related to the intent of how a product should be built.

This is best achieved through the easily secured, single-file IPC-2581 digital product model (DPM) design data exchange format. The digital engineering solution then assigns assembly work required in the design to any capable production configuration, often on demand, which meets the changing customer need. Lines selected to make the product need to receive a reliable standard form of information with which the machines can be easily and quickly prepared without the need for lengthy teaching, learning, or any significant data translation.

The combination of the IPC-2591 Connected Factory Exchange (CFX) standard and the IPC DPM achieves this with the digital engineering solution providing the necessary environment and tools. The digital MES also utilizes CFX to create visibility of production status and events so that available line configuration opportunities can be identified. This is done with consideration of live optimization of the overall factory and product flow as well as of the supply-chain material availability and logistics to and from machines. The net result is the ability to execute a production job from receipt of design to the start of manufacturing on any line configuration in a mere fraction of the time traditionally required, eliminating much of the manufacturing downtime associated with process preparation.

The opportunity for design is created from this new assembly digital engineering paradigm. What happens in the process of assembling a product has great value in the assessment of the design itself in terms of product quality—both during assembly and in the market—as well as long-term reliability. The use of IPC CFX and DPM standards as part of the digital MES environment means that data related to the choice of materials, process settings, test measurements, etc., can be gathered far more quickly, accurately, and consistently.

Further, the direct correlation of data from each specific manufacturing fragment back to design revision enables the discovery of factors that affect real-world product performance, which can be influenced by design. Examples include the consideration of different materials that may be used, including control and restriction of materials, as well as the knowledge of differing process strengths and challenges to ensure a greater degree of testability and reduction of failure opportunity.



Variation and change represent both cost and risk to assembly manufacturing, yet the trend is firmly established in this direction. The visibility of fragmented manufacturing needs to be clearly understood as it happens. There is no longer the opportunity to spend days and weeks of industrial engineering activity, optimizing the operation of a long-term, high-volume line. It is not beyond human ability to optimize defragmented production; we just need a little help.

Using IPC standards, having a direct digital path for data flow from design through digital MES and then back to design has eliminated the variability of unknown, drawn-out events. In turn, we are creating an improvement opportunity for design, planning, and engineering for Industry 4.0 to operate effectively in a highly fragmented and volatile manufacturing operation. The gap between design and manufacturing is an order of magnitude narrower and clearer now, leading the way for the opportunity to optimize design for easier and quicker manufacturing with greatly enhanced quality and reliability. Design is a key part of—and benefits from—Industry 4.0.

The use of IPC standards means that the traditional barriers to advancement are removed. These include barriers caused by system and machine incompatibility that bring the need for manual intervention and associated loss of data integrity. If you are not utilizing the latest generation of digital IPC standards together with a modern digital MES solution within manufacturing, then you are missing the value from the technologies and best practices that they represent.

It's time to revisit the IPC-2581 digital product mode as well as the new IPC CFX and start to discuss the real business opportunities that they represent in terms of the whole breadth of the design and assembly business. These technologies are analogous to the move from a mechanical hard disk to a solid-state drive (SSD), and in the near future, choosing to do your shopping online. Gotta keep up! **DESIGN007**

Michael Ford is the senior director of emerging industry strategy for Aegis Software. To read past columns or contact Ford, click here.

Automation and the Smart Factory: Introduction to Industry 4.0

Feature by Happy Holden
I-CONNECT007

There's a lot of talk about automation, but I find that there is very little available on automation planning. This is one of my specialties. I started by studying for an MSEE in control theory, which went well with my bachelor's degree in chemical engineering because I specialized in process control and IC manufacturing.

Before we get started, remember that the benefits will be derived only if certain cardinal principles are observed. This article briefly outlines the background of computer-integrated manufacturing (CIM) and its evolution to Industry 4.0 and smart factories.

The characteristics of successful automation application in manufacturing depend on how well business and technical management understand and promote the strategies, tactics, and philosophies used in modern manufacturing. Successful automation implementation can be enhanced in any company, small or large, by reviewing the philosophies of CIM, automation, management roles, mechanization, SPC, TQC, Lean, MRP, and DFM.

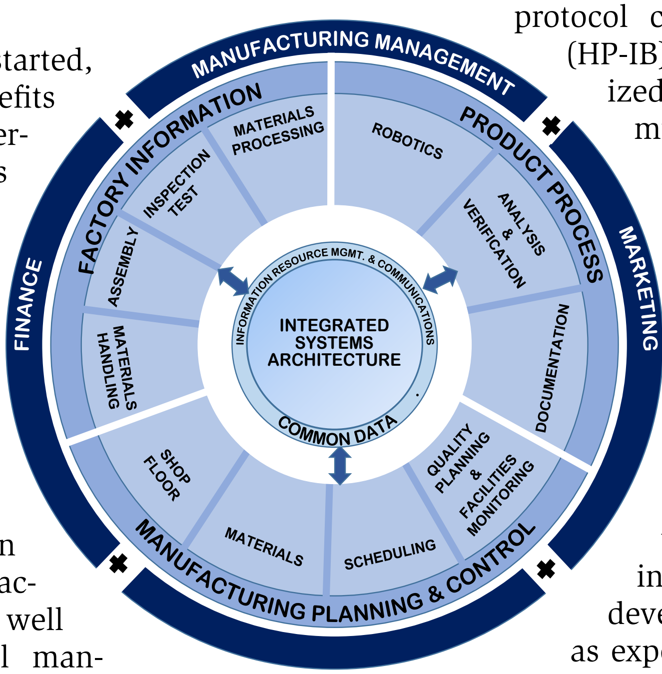


Figure 1: The CIM wheel defined by CASA/SME.

Computer-Integrated Manufacturing (CIM)

The strategies outlined here are considered CIM, but the current vocabulary now is "Industry 4.0" or "smart factories." Products include various software, computer, networking, interface, and measurement systems. At that time, HP had been in the automation business longer than any other company. It all started with requests from the government and others for automated test and measurement systems. Because of the need to automate various measurement instruments and systems, HP created the first machine-to-machine, plug-and-play protocol called HP Interface Bus (HP-IB). This was later formalized into the IEEE-488 communication standard.

CIM architecture was defined as early as 1980 when the CASA/SME published a presentation of computer-integrated manufacturing to provide a common set of terms for its members. The ring surrounding the wheel represents various influencing factors for the development of CIM such as expertise as a human factor, productivity as an economic factor, and computer technology as a technological factor.

The wheel itself contains four functions, including engineering design, manufacturing planning, production control, and factory automation (Figure 1). If the individual functions are connected to each other and operate with a common database, an integrated system architecture is created and represented by the hub of the wheel. This development has resulted in the realization that CIM, apart from

factory automation and functions, is indirectly related to the operational performance, such as design (product/process), and production planning and control.

Additionally, CIM is linked to common business administrative tasks such as manufacturing management, strategic planning, finance, marketing, and human resource management. A further innovation was the addition of information resource management and communications between the different functions. Therefore, a common database alone is insufficient for achieving integration. The all-embracing nature of the CIM wheel reflects the idea promoted by CASA/SME that CIM must be viewed as a concept embracing the company as a whole.

The Outer Ring

The common business administrative tasks related to CIM are located on the outer ring of the wheel. They primarily form the company's connection to the outside world. Data processing applications can be found in the most diverse areas. Most software systems applied in these areas were originally self-styled developments, which are increasingly being replaced with standard commercial software packages. Currently, this software is installed primarily on mainframes. Overlaps of its functionality exist mainly with the software of the production planning and control.

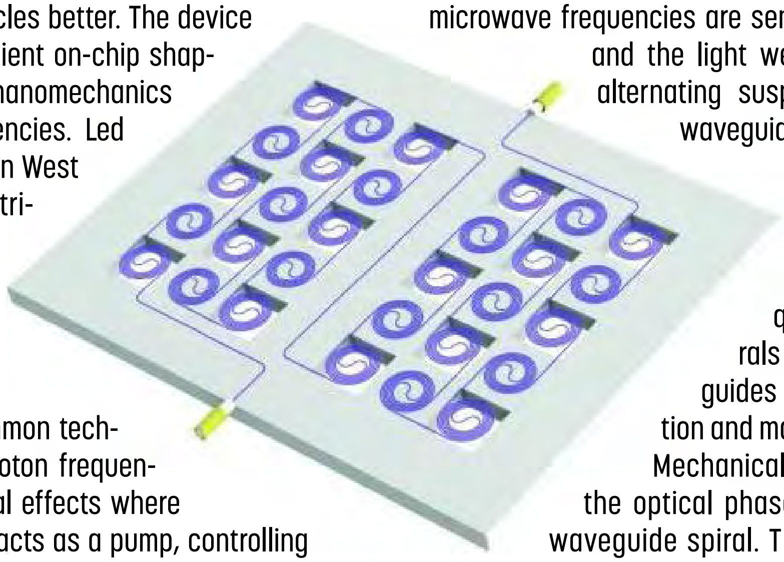
The Inner Ring

Functions related to the operational performance of the company are located on the inner ring of the wheel. Data processing applications for the development and design area are CAD simulations; analysis programs, such as the finite element method (FEM); and drawing storage and management, such as group technology (GT). **DESIGN007**

To read the rest of this article, which appeared in the March 2019 issue of *SMT007 Magazine*, click here.

Photonics Breakthrough: Device That Shakes Light

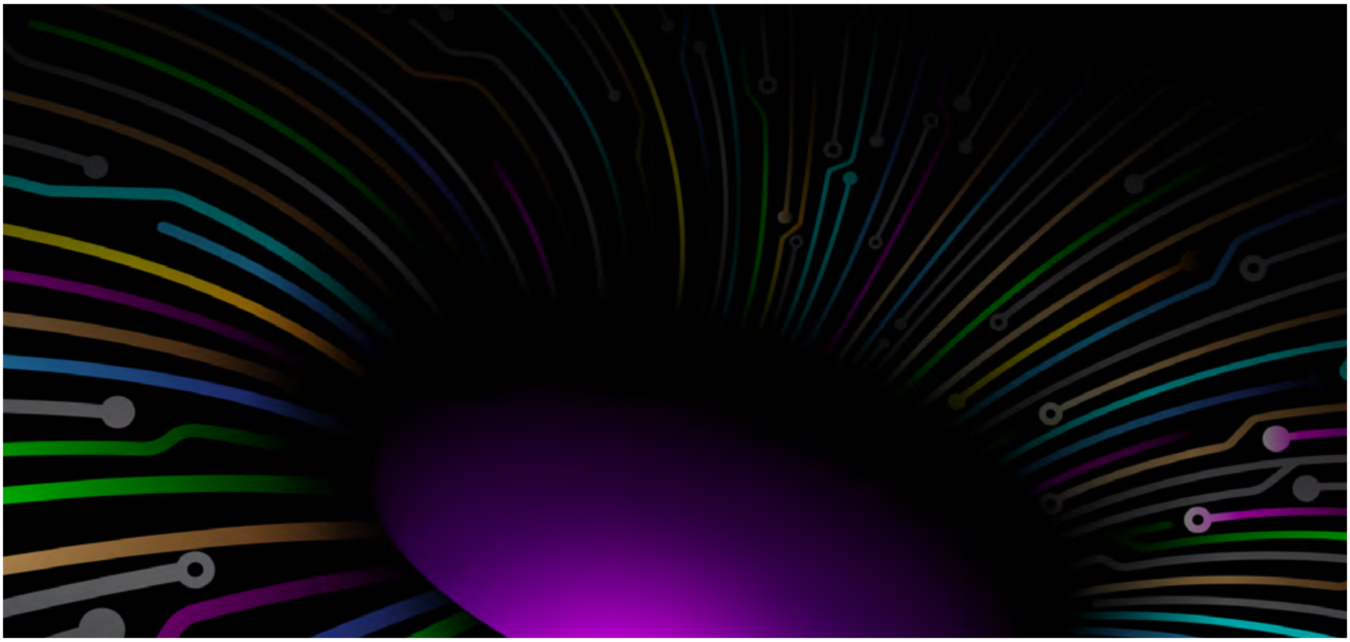
Researchers at Yale University have developed a device that combines mechanical vibration and optical fields to control light particles better. The device has demonstrated an efficient on-chip shaping of photons enabled by nanomechanics driven at microwave frequencies. Led by Hong Tang—the Llewellyn West Jones, Jr. Professor of Electrical Engineering, Applied Physics, and Physics—the results of their work are published in *Nature Photonics*.



Currently, the most common technique for manipulating photon frequency is with nonlinear optical effects where a strong laser essentially acts as a pump, controlling the color and pulse shape of a signal photon by providing extra photons to mix with the original one. However, the effect is weak, so the process requires a very strong laser, which creates noise.

To break these limits, the Yale researchers created a device that consists of a series of waveguides. Light and microwave frequencies are sent through the device, and the light wends its way through alternating suspended and clamped waveguides on a single chip. This creates a positive and negative effect, corresponding to the microwave frequency. The light spirals in each of the waveguides to prolong the interaction and maximize efficiency.

Mechanical vibrations modulate the optical phase in each suspended waveguide spiral. The mechanical vibrations essentially shake the photons, dispersing them as if they were grains of sand. This accumulates to generate what's known as deep phase modulation. (Source: Yale University)



XNC Format: Gerber Takes Data Into the Future

Feature by Denis Morin, Karel Tavernier, Jean-Pierre Charras, and Marius Matioc
UCAMCO, KICAD AND PENTALOGIX

Gerber is the world's favourite data exchange format for PCB image data: it's easy to use, crystal clear, and gives designers and engineers an unequivocal language with which to communicate with each other. And this grand, old man of the PCB industry has remained at the forefront, powered by ongoing developments that add capability and functionality without ever compromising its characteristic simplicity and ease of use.

It's the ideal solution for transferring drill data too, as can be seen from scanning the specification. And many in the PCB industry use it for just this, but the majority are still transferring their routing and drilling coordinates using NC formats. These were never designed for data transfer, and more often than not create confusion and waste time.

Some argue that Gerber files, unlike NC files, can't be sent to a drilling machine. True enough, but PCB manufacturers never send their clients' incoming files to their machines anyway. Instead, the data goes through the CAM process and is then altered and output as is appropriate to the manufacturer's specific production line. For CAD, the question should not be which format is best for the machines, but rather which format is best for input into CAM. As we've said, this is undoubtedly Gerber.

So, why are CAD developers and their users still stuck on NC formats? It's most likely a question of inertia or tradition. Drill information has been transferred for decades using NC formats, principally Excellon, that are similar to the 1985 IPC-NC349 specification. Also, there's still a lot of legacy software out there, so NC files will likely be with us for a while.

The Problem With Existing NC Specifications

The problem is that so many NC files are of deplorable quality because the NC format was never designed as a data transfer format. It has always been a machine driver and contains all sorts of information that a drilling machine needs, but that is irrelevant and confusing for data exchange. For example, CAD software will typically ask users to specify whether routing should be achieved using nibbling or slot creation and which drill feeds and speeds are to

IT-170GRA1

IT-170GRA1 Value Proposition

- Halogen Free
- Best in class performance in its space
- Best in class CAF performance
- Very attractive price to performance ratio
- Pass MRT-6 requirements
  - -CAF > 1000 hours
  - -0.65mm pitch equivalent, no thermal issue
- Available with RTF and 2μ copper which provides additional performance on a very solid platform
- Df = 0.0075 @10GHz

Intel Purley Mid-Loss Solution – IT-170GRA1

Futures

Halogen free mid loss, Df < 0.01
Tg 180ºC by DSC, low CTE

Applications

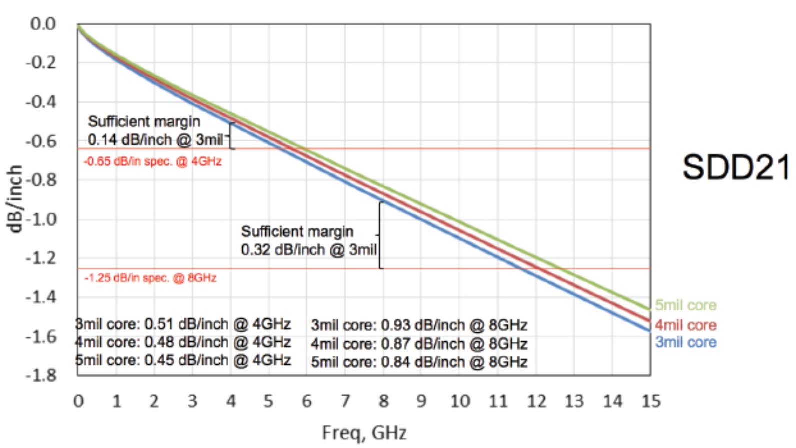
Server/Storage/Switch (10G, 40G)
Backplane, Telecom
Base station

Feature *Purley Platform Mid-Loss Solution – Hi Tg*

General Properties

Items	Methods	IT-170GRA1
Tg (℃)	DSC	180
T-288 (w/ 1 Oz Cu, min)	TMA	60+
Td-5%(℃)	TGA 5% loss	380
CTE (%), 50-260℃	TMA	2.4
Peel strength (lb/inch)	1 oz	7.0
Water absorption	D-24/23	0.1
Dk: 2-10 GHz	Bereskin	3.96 – 3.99
Df: 2-10 GHz	Bereskin	0.0073 - 0.0075

IT-170GRA1 Insertion Loss



ITEQ

be used. These are decisions that only the fabricator can make, and yet many CAD professionals will feel duty bound to give some sort of answer, which will inevitably be wrong.

Clearly, CAD developers will try to avoid such scenarios by going through their chosen NC format and picking what they believe is most appropriate for their software and the CAD to CAM data transfer process. This is not easy, as the language is dense, sometimes redundant, and IPC-NC349 and Excellon 2 contain legacy Excellon 1 code—most of which CAD developers don't need. So, for fear of leaving out parts of the format that could be of value, developers tend to include more than necessary, which just adds more confusion for the CAD user.

Despite the developers' best efforts, it's not always clear how to use parts of the NC formats or if they are even capable of transferring certain data. CAD users will simply leave these parts out of their drill files and express the relevant information as sidecar information in comments or in separate text files.

But the biggest problem with these NC specifications is that, thanks to an age-old space-saving convention, the drilling coordinates lack a decimal point. That's okay if there's a command or header in the file that indicates where the decimal point must be—the so-called fixed "point format." But in Excellon files, there is no such instruction or standard for saying where it should be, so designers are on their own. Similarly, there is no standard for expressing whether the designs are in imperial or metric measurements. The Excellon specification does mention defaults, but these are also confusing and can end up being used in different ways.

All of this places the final responsibility on the CAM engineer to try different possible variants until the drill files fit with the copper files. This is fine—if not great—when handling normal boards, but is not okay when handling RF boards, for example, where there are no clear pads to fit the holes.

An additional issue in the NC stakes is that the specification is no longer published, so the industry has relied for decades on copies of copies that may be infringing copyright protections. And the IPCNC-349 specification—which is dense, overcomplicated, and

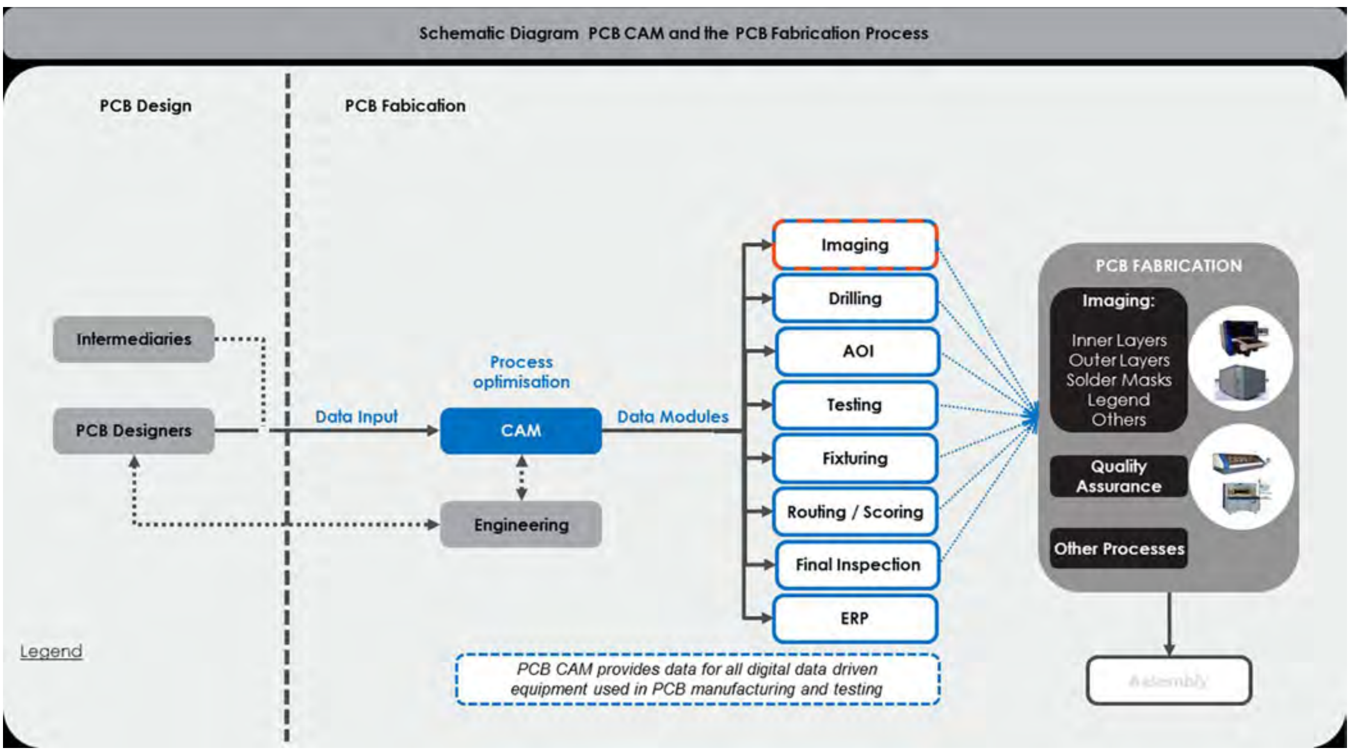


Figure 1: An example of the many steps of the process from PCB design to manufacturing.


U.S.C.

full of overlapping methodologies—is hardly in circulation because it's expensive. So, ironically, the PCB industry is likely developing NC files based on non-existent, illegal, incomprehensible, or unaffordable specifications. And when it's not, CAD software is reverse engineered from the clutter of existing NC files.

XNC

So, where do we go now as an industry, given that we're not yet ready for Gerber drill files? Fortunately, there's a new format for PCB drill data that takes all the confusion out of CAD software development and the CAD-to-CAM drill data exchange process. Designed by Ucamco, KiCad, and PentaLogix with the support of Graphicode, Cuprum, and ZofzPCB, XNC is a strict subset of the widely used NC format.

We believe that the first step towards improving the NC drill chaos is to develop a simple, clear specification without embellishments—one based on an existing format that can be read by all decent PCB drill input software. To this end, we have taken great care to design the CAD/CAM Exchange NC (XNC) format—a complete, compact, and unequivocal subset of IPC-NC-349 that is capable of exchanging CAD/CAM drill information without the need for additional sidecar files.

And we've added to this the power of Gerber-type metadata or attributes. XNC attributes can be attached to the complete file, tools, or individual holes, describing characteristics in a standard, flexible way using similar syntax to that used for Gerber attributes. XNC files are compatible with Gerber X2 and can be added seamlessly to X2 data sets while also ensuring that the format is compatible with software that does not read attributes.

With XNC, CAD developers can create output software easily and quickly, using formats that are already well known but without the headache of having to wade through and choose from a bewildering array of possibilities and functionalities, or reverse engineer from multiple incomplete and confusing NC files. We guarantee that if CAD developers limit themselves to using just the XNC format, they will give their clients exactly what they need—a tight file format that will improve the CAD-CAM data transfer process overnight, and an NC reference towards which the industry can work so that NC files converge to a common standard.

Conclusion

Existing NC drill data CAD-CAM transfer processes are deeply flawed thanks to confusion at every level of the CAD and CAM information development process due to industry inertia and inappropriate data format specifications. A lot of time and resources are being wasted by CAD software developers trying to make sure that every eventuality has been accounted for in their software, CAD professionals delivering irrelevant and non-standard information about their designs, and CAM engineers interpreting the results. A new drill data exchange specification designed by some of the industry's leading PCB software providers and based on an existing and known NC format promises to alleviate many of the issues and pave the way to a new industry standard for NC formatting and files.

The first version of the specification of the XNC format can be found here. DESIGN007

Karel Tavernier is the managing director of Ucamco with 30 years of experience in software and imaging equipment.

Denis Morin is a software application engineer on Ucamco's European support team.

Jean-Pierre Charras is the founder of KiCad, researcher at Laboratoire des Images et des Signaux, and a professor in electronics engineering and image processing at IUT in France.

Marius Matioc is the creator of Lavenir CAM software and head of product development at PentaLogix.

XPLM: Using PLM to Integrate ECAD and MCAD Data

Feature Interview by Andy Shaughnessy
I-CONNECT007

During AltiumLive in Munich, I met with Robert Huxel, XPLM's director of business development for EMEA and APAC. XPLM offers data integration for some of the big EDA tool companies, and their tools can integrate ECAD and MCAD data into PLM systems. I asked Robert to tell us about the requirements of today's PLM tools, the changing world of ECAD and MCAD integration, and whether these two types of data are ever going to converge.

Andy Shaughnessy: Good morning, Robert. Can you tell us a little about XPLM?

Robert Huxel: XPLM is one of the most popular providers of integration between engineering applications and PLM systems. And if I'm going to talk about engineering applications or authoring tools, we are talking about mechanical design, electronic design, electrical design, software, simulation, and some other tasks.

Meanwhile, you have the business world. We're talking about the life-cycle management area. Product management means that these disciplines of the engineering side must somewhere come together to build up a project, and a project doesn't consist of just an enclosure or a PCB or a cable; it is a combination of all of them.

Years ago, at the very beginning of this upcoming world of PLM systems, the integration from mechanical applications was popular. Every mid-range and high-end company wanted to have an integration of their ECAD data to MCAD to the PLM world. That's where XPLM came from around 15 years ago—integrating those types of applications—followed by electrical cable and harness design. Today, many companies demand an integration from ECAD tools to the PLM world. For ECAD tools, we are talking about Altium, Cadence, Mentor, and many more.

Shaughnessy: I understand that you're partnering with PTC also.

Huxel: Exactly. PTC is quite a special partner. PTC had their own ECAD integration and they "sunset" this integration. Now, XPLM is the qualified partner for making integrations be-

tween the ECAD world and PTC, the Windchill software PLM system.

Shaughnessy: Who is a typical type of customer for XPLM? We would think of automotive, because of all the different types of legacy data.

Huxel: I have seen so many companies, even in the automotive industry, that do not have a PLM system. Now, the automotive industry is forcing their Tier 2 customers with PLM systems already in place to identify which part is built in which series of each car. And yes, typically, our customers are across all the domains—not just automotive. It is really going across all areas, such as medical and aerospace too. All of these industries are affected by that.

Many companies today have a PLM system. I do not want to say that this market is settled, but the high-level companies have at least one PLM system, and most of the large companies are doing electronics today—not only mechanics or electrical or software—which is why the demand becomes more and more. Integrating an ECAD system is a little bit more complicated than just a mechanical thing—an enclosure. It is one thing. Like a screw is a screw is a screw, but a PCB consists of far more data. It's not only the native data and what the authoring tool can read and write; it's also the created and generic data for manufacturing.

Shaughnessy: And even terms are different from country to country or company to company, such as "template." Other countries and companies may have a different term for the same thing.

Huxel: Absolutely. With the ECAD world, it uses a totally different language.

Shaughnessy: And with PLM, there's this big component shortage with some discretes being almost impossible to find now. You look for them, and they have 50- or 80-week lead times. It seems like this would be a really handy thing.

Huxel: Right. Going from the component level, thousands of components are introduced every day. Some of them have reached the end of life because they're antiquated, obsolete, etc. It depends on the structure and culture of the company where this kind of data is stored. It is very often stored in a PLM system, but there are also other techniques around. Web-based platforms provide this kind of information too, and it depends on how a company is structured. If this information is tied to the PLM system and synchronized with the ECAD world, it has direct integration into the ECAD tools.

Shaughnessy: That sounds like kind of a brave new world if you can integrate the two because they both developed separately for so long.

Huxel: Right. MCAD would be way closer to a PLM than ECAD, even today. But the ECAD integrations have been around for more than 25 years. They had been on the market since that time, but the demand from the industry hadn't been really high. In the early days, adopters had been high-end companies; today, we're going down to the standard of 1,000-employee companies and smaller. Because they all have time pressure, they have to follow the time-to-market rules and stuff like that, and they need to identify what happened to specific data and make sure everything is in order to trail backward.

Shaughnessy: When you're selling, you're selling to the management; you're not selling to the PCB designer or design engineer. You want the boss to see the value in this.

Huxel: Exactly. So, the electronics engineer wants to get rid of additional work. Clearly, integration is not cheap, and it is not free. We have to talk to management.

Shaughnessy: Great. Thanks for speaking with me, Robert.

Huxel: Thank you, Andy. DESIGN007

PCB007 Highlights

Flex Talk: Don't Build Flex That Doesn't Flex ▶

One of the primary advantages of moving to a flexible circuit design from a rigid board is the ability to package the flex in three dimensions, bending or folding into imaginative configurations and saving precious space in the final package.

It's Only Common Sense: So Long, Marty ▶

Let me tell you about my good friend Marty Petersen. He was one of the most intriguing people I have ever met and had the pleasure to work with. Marty was always all in, whatever task he undertook. When I met him, he was handling the purchasing for us at Automated Systems, the PCB shop we both worked at just outside of Milwaukee.

Insulectro Sees Growth and Opportunities in Printed Electronics ▶

Judy Warner speaks with Tim Redfern, Insulectro president, and Kevin M. Miller, VP of sales, about growth in the printed electronics market, the direction Insulectro is going, and opportunities for North American PCB suppliers. They note that the company will increase their focus and investment in the printed electronics market.

Ventec at APEC 2019: Thermal Management and IMS Solutions for Power Electronics ▶

Ventec International Group will showcase Ventec's latest power electronics PCB material technology innovations at APEC 2019, which is taking place at the Anaheim Convention Center from March 18–20 in Anaheim, California, USA.

Institute of Circuit Technology Evening Seminar ▶

The Institute of Circuit Technology hosted its first 2019 seminar at the Woodland Grange Hotel in Royal Leamington Spa in the Midlands of England on February 26. The diverse programme of four presentations was introduced by ICT Chairman Andy Cobley, a professor at Coventry University, who stood in for Bill Wilkie, who had been taken ill at short notice.

The Right Approach: Industry 5.0—Can We Learn From Other Industries? ▶

The last few IPC APEX EXPO events have focused heavily on Industry 4.0, which is all about the Internet of Things (IoT), automation, and data exchange between machines.

Inspiring the Next Generation of Industry Leaders: IPC STEM Student Outreach Program ▶

At IPC APEX EXPO 2019, I-Connect007 Managing Editor Patty Goldman spoke with Colette Buscemi, IPC's senior director for education programs, about the success and expansion of the IPC STEM Student Outreach Program, activities and scholarship opportunities for students through sponsor support—including I-Connect007—and feedback she received on the event.

Isola Executive Vice Chairman and Acting CEO Travis Kelly on the Upcoming Year ▶

Isola Executive Vice Chairman and Acting CEO Travis Kelly discusses the recent milestones for the company, including the leadership transition. Travis also outlines his agenda for the upcoming year and gives an update on Isola's new facility in Chandler, Arizona.

San Diego Chapter Updates and More

The Digital Layout

by Stephen Chavez, CIT, CID/CID+, IPC DESIGNERS COUNCIL

This month's column is packed with recent activities, including a spotlight on the San Diego Chapter and an interview with Luke Hausherr, the new chapter president. You'll also find an update from the IPC Designers Council Executive Board as collaboration with the new IPC Education Foundation continues to evolve and recommended reading featuring an interview with a young designer.

Chapter Spotlight

by Luke Hausherr, CID+
SAN DIEGO CHAPTER

On March 12, the San Diego Chapter hosted our first meeting of the year. Presenter Michael Goode discussed IC package design. It was a very informative meeting, and we learned a lot about the different types of IC package design and how it is done. The audience was very engaged with over 25 people in attendance.

We also hosted our officer elections. Here are the newly elected officials for the San Diego Chapter:

- Luke Hausherr, chairman (president)
- Ben Savage, vice chairman
- Bill Gebhardt, treasurer
- Judy Warner, education director
- John Carney, secretary
- Bob Griffith, member at large

Our chapter's plans for this year include:

- Working with the national IPC council to obtain more funding
- Creating a website for our chapter to attract new members
- Working with colleges and other avenues and existing connections to attract new members
- Hosting an event at the Del Mar Electronics and Manufacturing Show (DMEMS), our biggest event of the year

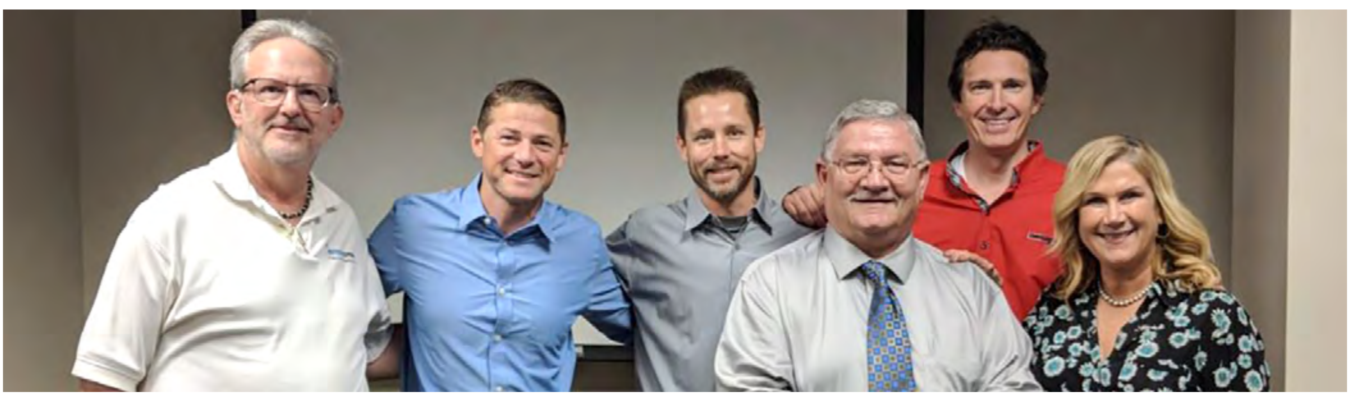


Figure 1: New San Diego Chapter leadership (L-R, back row: Bill Gebhardt, Ben Savage, Luke Hausherr, John Carney; front row: Bob Griffith, Judy Warner).

As usual, the chapter meeting ended with a raffle giveaway where many people won prizes to take home. I'd also like to thank San Diego Chapter members and the new leadership team for all of their support as I take on this new role and hope to contribute to the success of the chapter. Our next chapter meeting will take place at the DMEMS on May 1.

Feature Interview

by Duane Benson
SCREAMING CIRCUITS
I-CONNECT007 COLUMNIST


Duane Benson

San Diego PCB and Screaming Circuits are both divisions of Milwaukee Electronics headquartered in San Diego, California, with offices in Phoenix, Arizona, and Milwaukee, Wisconsin. As marketing manager and CTO at Screaming Circuits, I interviewed Luke Hausherr, senior PCB designer at San Diego PCB and newly elected San Diego Chapter president, about his vision for the chapter. Luke was also elected to the IPC DC Executive Board on March 11, which he views as an important position for the San Diego Chapter because it will help provide more local representation.

Duane Benson: Congratulations on your new roles with the IPC Designers Council. How long have you been active in the IPC DC?

Luke Hausherr: In 2012, I was elected secretary of our local San Diego Chapter. This year, I was nominated and elected to become the president of our chapter to replace Bob Griffith who had served since 2007. At the same time, I was also nominated to become a member of the IPC Executive Designers Council, which is an important role. By being both the president of my local San Diego Chapter and a member of the IPC DC Executive Board, I will be able to better serve both my chapter and the IPC DC. I can help integrate local chapter efforts and resources from IPC to serve our San Diego design community. I hope to be a more effective voice while representing our local chapter on the national level; it's a great opportunity.

I've always used IPC standards to add quality and reliability to my designs. I received my CID certification after being in the industry for two years back in 2006, which increased not only my knowledge for fabrication and assembly but also my confidence and skills to advance to a more senior-level designer rapidly. I've been active in the San Diego Chapter for about seven years now, but I've been involved with IPC since the start of my career over 15 years ago.

Benson: What made you decide to join leadership?

Hausherr: I attended San Diego Chapter meetings since the start of my career, and I was always interested in getting more engaged. When the opportunity arose to join as secretary, I eagerly took on the role. I immediately started trying to locate all of the PCB designers in San Diego to invite them in our chapter events and increase attendance at our local meetings held 4–6 times throughout the year.

Benson: How do you think you can have an impact on the IPC DC?

Hausherr: I am extremely passionate about design and always eager to increase our membership as well as engage the community by helping spread information about design resources. I love meeting new designers and learning about technologies and advancements in our industry.

Benson: Do you have any specific goals for the San Diego Chapter?

Hausherr: My goals have been and always will be to engage as many designers through our chapter as possible. I also want to utilize my position on the Executive Board to leverage resources to deliver a variety of presentations from powerhouse keynote speakers and industry leaders available at our chapter meetings.

Figure 2: San Diego DC Chapter members Ben Savage (L) and Luke Hausherr (R) look on as Bob Griffith makes a point.

Benson: What's the primary benefit that the IPC DC brings to your design community?

Hausherr: Since there are very few educators and resources for designers to continue to grow in their knowledge of technologies and advancements in the industry, the primary benefit is education. I've learned more from industry leaders at these events than in 15 years of designing in my profession alone. This organization allows people who may be captive or in a bubble to engage in real-life demonstrations of new materials, equipment, technologies, and practices. We also learn about things from different professions and perspectives in the industry so that we can better understand electronics manufacturing as a whole.

There's always room for improvement, but if there isn't any guidance on how to improve specifically, unfortunately, we can become stagnant, or even worse, become accustomed to producing and performing subpar practices and not even realize it. Everyone in the industry can benefit from being a part of an IPC DC chapter; it serves as a great learning and networking opportunity for anyone from sales to engineering. If there is anyone out there that would like to get involved with the San Diego Chapter or just learn more about our organization, please feel free to email us at ipcdc.sd@gmail.com.

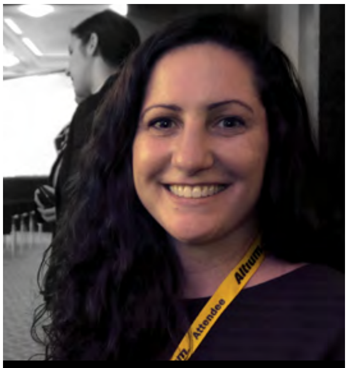
Luke Hausherr has over 15 years of industry experience and has worked on hundreds of designs throughout his career for a variety of companies and end usage. Luke has designed projects ranging from analog, high-speed RF, and dense high-speed digital boards for various applications, such as aerospace, automotive, military, medical, IoT, and more. He has trained many PCB designers, supervised design teams, and written numerous training documents. In addition to his leadership positions with the San Diego Chapter and IPC DC Executive Board, Luke also serves on the advisory committee for the mechanical/drafting department at Palomar Community College.

IPC DC Executive Board

On March 11, the IPC DC Executive Board had its initial meeting with the new IPC Education Foundation to discuss collaboration moving forward. The bulk of the meeting was spent roadmapping. Due to the complexity and individual time constraints with everyone involved, a follow-up meeting was held on March 21 to continue working on the roadmap activities. Stay tuned for further updates.

Recommended Reading

In the spirit of continuing to highlight positive activities, especially when it comes to fellow designers in our industry, the recent-



Nicole Pacino

ly published interview with Nicole Pacino, team lead of Cobham, a defense contractor, by Design007 Managing Editor Andy Shaughnessy is a highly recommended read indeed. The interview took place at AltiumLive in Munich and discusses how Nicole (the newer generation of PCB designers) became involved with PCB design at an early age, being heavily influenced and mentored by her father, Mike Creeden, MIT, CID+. Nicole, like other designers in the industry, has grown to have a very fruitful career as a PCB designer. She closes the interview with her advice for new designers and explains how she stays up to date on the industry and pursues continued professional development.

2019 Training and Certification Schedule

IPC Certified Interconnect Designer (CID)

- April 22–25: Schaumburg, IL
- May 21–24: Pittsburgh, PA
- June 18–21: Kirkland, WA
- August 6–9: Baltimore, MD
- August 26–29: Markham, ON
- September 6–9: Santa Clara, CA
- September 19–22: Schaumburg, IL
- October 21–24: Anaheim, CA
- November 2–5: Raleigh, NC
- November 5–8: Dallas, TX

IPC Advanced Certified Interconnect Designer CID+

- April 16–19: Markham, ON
- September 6–9: Santa Clara, CA
- September 10–13: Kirkland, WA
- September 19–22: Schaumburg, IL
- October 21–24: Anaheim, CA
- November 2–5: Raleigh, NC
- December 3–6: Manchester, NH

Note: Dates and locations are subject to change. Contact EPTAC Corporation to check current dates and availability. A minimum enrollment of seven students is required for a class to be held.

PCB Design Events

Del Mar Electronics and Manufacturing Show (DMEMS)
- May 1–2: San Diego, CA
- manufacturing.show

PCB2Day
- Controlling noise, EMI, and signal integrity in high-speed circuits and PCBs
- April 17–18: Seattle, WA
- June 13–14: Boston (Chelmsford), MA
- pcb2day.com

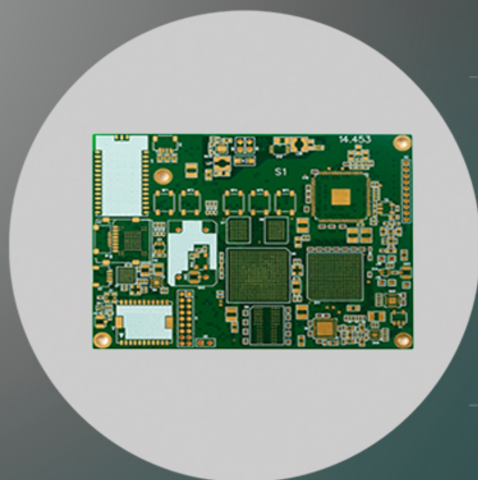
Realize LIVE
- June 10–13, 2019: Detroit, MI
- Realize LIVE

PCB West 2019
- September 9–11: Santa Clara, CA
- pcbwest.com

AltiumLive 2019
- October 9–11: San Diego, CA
- altium.com/live-conference

The IPC Designers Council is an international network of designers. Its mission is to promote printed circuit board design as a profession and to encourage, facilitate, and promote the exchange of information and integration of new design concepts through communications, seminars, workshops, and professional certification through a network of local chapters. **DESIGN007**

Stephen Chavez is a member of the IPC Designers Council Executive Board and chairman of the communications subcommittee. To read past columns or contact Chavez, click here.



Preparing for Tomorrow's Technology Today

Connect the Dots

by Bob Tise, SUNSTONE CIRCUITS

At a recent Sunstone Circuits planning summit, Matt Stevenson, VP of sales and marketing, and I led a wide-ranging discussion about emerging technologies and how they will impact PCB manufacturing (Figure 1). The following is an abridged transcript of this conversation.

Figure 1: Bob Tise (L) and Matt Stevenson (R) meet to discuss emerging technologies.

Which Industries Have the Most Innovative, New Technology?

Matt Stevenson: One industry we're seeing a change in is transportation electronics. Battery-powered vehicles, autonomously driven vehicles, additional sensors and gadgets, and a focus on Bluetooth use are all happening in the transportation industry more so now than ever. From a PCB manufacturer standpoint that's pretty exciting.

Bob Tise: There's also more complexity because of the functionality requirements. That makes it all the more important to ensure designs are manufacturable and that the boards will perform as needed in their operating environments.

Stevenson: Yes, and these electronics are continuously becoming smaller and faster. Vehicles require circuit boards that can withstand extreme temperatures, vibration, and dirt. After outer space, it's the most demanding environmental category there is. We need to design for big swings in temperature from Siberia to Dubai. Putting a car in the sun in some places in the world at 250°F (~120°C) is not unheard of in the cabin or under the hood (Figure 2). As more and more electronics are used to operate our cars, the devices in them keep getting smaller. Ensuring the devices do not trade durability for functionality and size is a big challenge for PCB designers and manufacturers.

Figure 2: Vehicles require circuit boards that can withstand extreme temperatures.

How Are PCB Manufacturers Meeting Challenges Like These?

Matt Stevenson

Stevenson: It is necessary to use materials—such as laminate, fiberglass, epoxy, thermoplastic—that work at the right speed, at the right temperature, and in the right condition. Each material has a specific range of electronic speed and stability in addition to the associated environmental concerns. To be a full-service automotive supplier, you must be able to support all of those needs at all times to produce robust, long-lasting boards.

Are You Witnessing Similar Trends in Other Industries?

Tise: Use of electronics is exploding in the health services industry as well. Because medical facilities are sterile, electronics used there must withstand exposure to chemicals needed to keep them clean. Any electronic used in a medical facility has to be completely encapsulated in a hardened plastic case, or it has to be disposable.

Stevenson: And because of the nature of their use, the devices have to be small and highly functional. There's a lot of innovation, but there are also challenges unique to the industry. In addition to what we've already discussed, it's important to remember every device used in the medical industry has to go through FDA requirements before it can be implemented, which means a multi-year test and validation process. That's a lot of iterating. So, if you're in that space, you depend on trusted partners to help you through that process.

What Are You Doing to Support Your Customers in the Healthcare Space?

Tise: We maintain standards of IPC-A-600 and IPC-6012, which are divided further into a Class rank. Class 3 is stringent. A customer wanting to reach Class 3 to have it be usable in the medical industry or anywhere else would need to design a top-shelf board. We help them get there.

Stevenson: Also, it takes multiple spins and revisions within the circuit board testing process as well as expert advice to catch design flaws and make modifications quickly. It helps to have a seasoned professional at hand to keep customers on track in their testing processes. That's a value-add service Sunstone Circuits provides to engineers.

How Are Robots Coming Into Play?

Stevenson: As robotics become mainstream in every industry, including automotive, medical, military, and with cameras and making movies; pretty much every vertical that you can think of is driven and made more commercial (Figure 3). Plus, it's really cool stuff! For the PCB industry, robotics represents both a business opportunity and a path to improving the manufacturing process itself.

Figure 3: Robotics are becoming mainstream in every industry.

Tise: And if you're an engineer responsible for designing and building a robot with a purpose, you know what you need in terms of functionality from a PCB. Designing the board is usually not an area of expertise, and that's where we can help. We coach customers to help them better design for manufacturability as well as build in features needed for an IPC Class 3 or 2 certifications.

Circuit boards aren't that complicated of a device, but there's complexity in designing them for durability, functionality, and manufacturability. The process of creating a circuit board is well established; it's the functionality that's new and exciting. These emerging technologies do things that haven't been done before and operate in environments new to electronics. When it comes to PCB design for these devices, the devil is in the details. That's our forte—paying attention to the details and advising customers to design a board we can produce that will work the way they need it to.

Figure 4: MakeHarvard's registered students getting ready to make.

What's Driving All of This Innovation?

Stevenson: Millennials and Generation Z are the driving force behind these emerging technologies. They may not be engineers or have classical training in all of the required disciplines, but they have an idea of how to interface hardware and software to solve a problem. They're getting their questions answered any way they possibly can—through social media or other self-serve channels—and they're making it happen quickly. They think outside of the box.

We've seen this with our work at MakeHarvard (Figure 4), which is an annual 24-hour hackathon competition open to U.S. undergraduate and graduate students that started in 2018. The students we've worked have come in with ideas to improve the world and the desire to learn how even if they don't have all the classical skills to begin with. MakeHarvard is a perfect place to find talent for that reason. These are the hires that may not have a resume or a job history yet, but they've been working in these fields and industries for years and are doing some cool things. They aren't constrained by corporate rules and regulations; they're passionate.

Tise: In the coming years, it will be interesting to see how this new blood will change the R&D departments at established companies. They are so procedurally oriented and often focused on a product's potential profitability as much as anything else.

Stevenson: Making profit is different than making innovation. We're seeing some customers focus on that profit, but innovation is necessary to keep up in these industries with so much new technology. **DESIGN007**

Read more about MakeHarvard in the March edition of *Design007 Magazine*.

Bob Tise is an engineer in PCB technical support at Sunstone Circuits. To read past columns by Sunstone or contact Tise, click here.

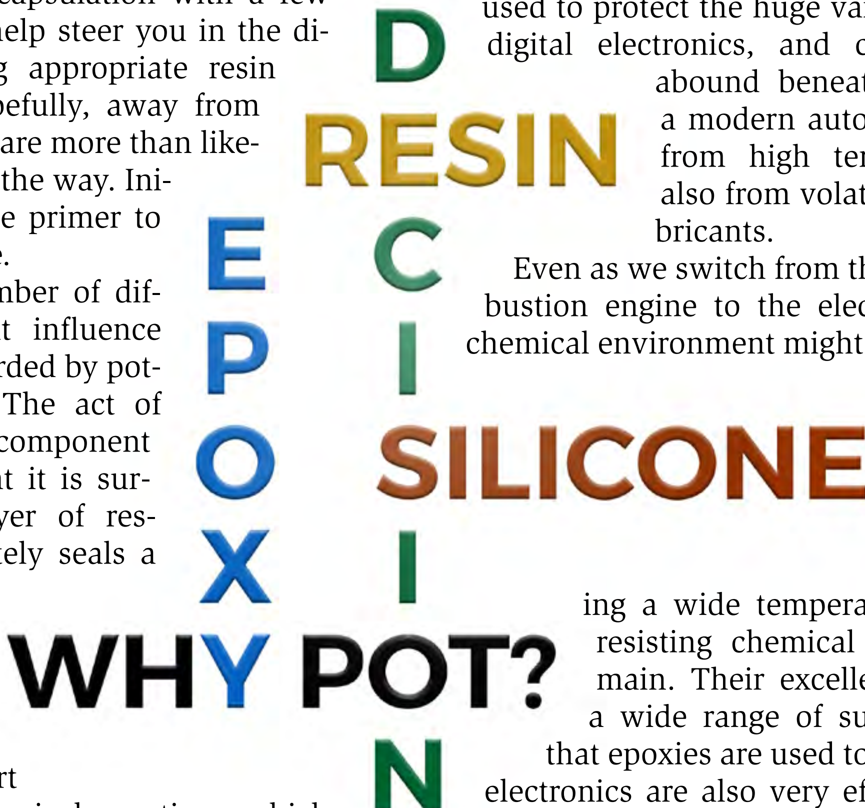
Five Tips to Further Improve Resin Encapsulant Performance

Sensible Design

by Alistair Little, ELECTROLUBE

In the second of my recent columns on resin potting and encapsulation, I will expand on my previous Q&A guide on the subject with further advice on selection and application.

Keeping to our tried and trusted five-point Q&A format, I am returning to the subject of potting and encapsulation with a few more pointers to help steer you in the direction of making appropriate resin choices—and, hopefully, away from problems that you are more than likely to encounter on the way. Initially, here's a little primer to whet your appetite.



There are a number of different factors that influence the protection afforded by potting compounds. The act of encapsulating a component or PCB means that it is surrounded by a layer of resin, which completely seals a component or an entire PCB from the environment in which it operates. When mixed, a two-part resin starts a chemical reaction, which results in the resin becoming fully polymerised to provide a homogenous layer. The polymerisation reaction creates a three-dimensional structure, which provides a barrier against chemical attack and high humidity, physical shocks, and the potentially destructive effects of thermal cycling.

Now, let's refer to our questions.

1. What typical applications use epoxy resins?

Epoxies are typically used where extremes of temperature and chemically aggressive environments are encountered. Under-hood applications are common, and epoxies are often used to protect the huge variety of sensors, digital electronics, and connectors that abound beneath the hood of a modern automobile not just from high temperatures but also from volatile fuels and lubricants.

Even as we switch from the internal combustion engine to the electric motor, the chemical environment might change, but the requirements for chemically resistant potting resins capable of tolerating a wide temperature range and resisting chemical attack will remain. Their excellent adhesion to a wide range of substrates means that epoxies are used to ensure that the electronics are also very effectively sealed against the external environment and are perfectly adapted for use in equipment destined for deployment in ATEX and other hazardous areas.

2. What typical applications use silicones?

Silicones are used where extremes of temperatures are to be expected, or the components

are temperature sensitive and would not survive the exothermic reactions that occur when two-part epoxies and polyurethanes are mixed and cured; this is particularly so when a large volume of material is needed for pouring into a single unit. Silicones are also suitable for applications where a high degree of flexibility is required, such as on flexible PCBs, and unlike epoxies, are easy to remove if circuit modifications or repairs are required.

Silicone resins have the broadest continuous operating temperature range of any of the available resin chemistries, so they are a natural choice for both high- and low-temperature applications. They maintain their flexibility over this temperature range with very little signs of degradation over time. Due to their high flexibility, they place very low stresses on delicate components, particularly those with weak and fragile connecting legs.

However, there is a downside to silicones, particularly the effectiveness of their adhesion to certain substrates. Moreover, their chemical resistance is not as good as that provided by an epoxy resin. Another category of resins—polyurethanes—would be the better choice for applications operating in the -30°C to +120°C region because they offer similar levels of flexibility and better adhesion to many substrates.

There is a downside to silicones, particularly the effectiveness of their adhesion to certain substrates.

3. What key pain points are associated with resin selection?

Resin selection is the art of compromise; it is deciding which characteristic or property of the resin is more important to your application compared with those previously outlined. Often, the main areas of potential problems lie in deciding what are the realistic maximum and minimum requirements compared, for instance, to the design limits, which are likely to include large safety margins.

Viscosity is another property that must be considered. Normally, where the lowest mixed viscosity resin is desired to promote excellent flow and coverage, there are thixotropic resins that behave somewhat differently in that their viscosity increases rapidly after mixing. This apparent change should not be confused with curing. The resin is still able to flow and has a useable life after it has stopped moving before reaching a final cure.

4. How do I overcome these pain points?

In most cases, many of the potential sticking points come down to the design brief and discussion between the designers and engineers as to what is feasible. If the high and low temperatures are only needed for a short period of time on an infrequent basis, and the normal operating temperature range is more modest, then this often opens up the choice to a much wider range of resins.

Similarly, when considering chemical resistance, determine whether the resin is actually the primary point of exposure. For example, if an LED is potted with an optically clear resin, but then a plastic cover with a gasket is placed over the top of it, then the level of protection that the resin needs to provide is significantly reduced. Although it delivers the primary electrical insulation layer, it is only providing a secondary barrier against the environment.

5. To pot or not to pot? Why do we pot?

Naturally, we would recommend that all electronic components—boards and units—be either coated or potted to extend the life of the finished unit and protect the components against the environment. The level of protection required depends on the environment to which the finished unit may become exposed. It might be indoors in a domestic setting where a light layer of dust might be expected. Contrast that with a unit submerged in a garden pond for four months of the year, or one that is located in a hazardous industrial environment. Some units may potentially be used undersea for 20+ years or positioned on an aircraft subject to short-haul commuter routes with regular temperature and pressure variations. Other units may be exposed to the vacuum, extremely low temperatures, and ionising radiation hazards of outer space; the variations are endless.

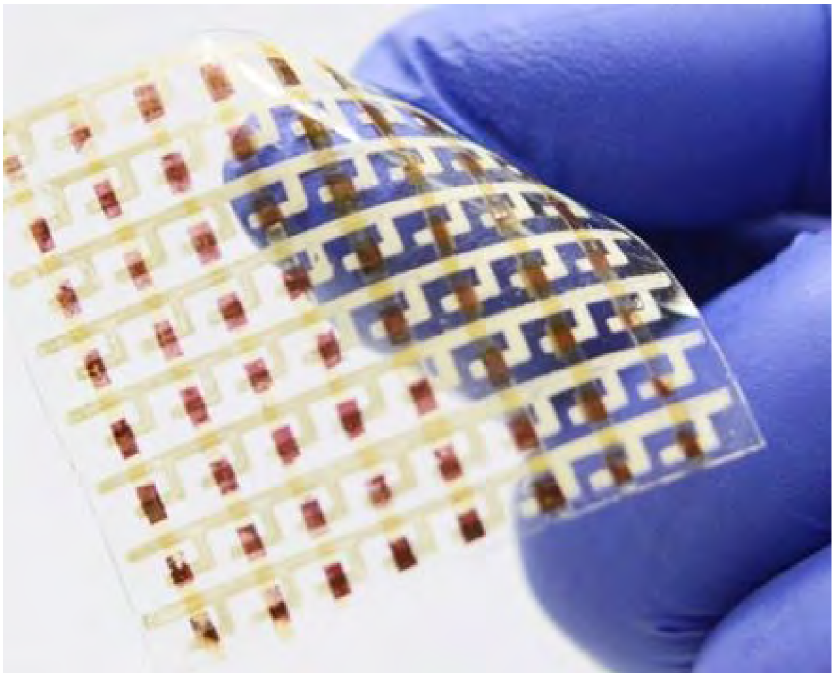
Under less extreme conditions, you might ask, "Is a resin still the best option, or should a coating be considered as an alternative?" This is an interesting point because the protection provided by a coating offers a number of advantages over the application of a resin. However, as always, the choice will depend on what level of protection the designer requires. In addition, if you need to protect your intellectual property and avoid the underlying circuit being copied, then a resin will not only provide excellent protection due to its toughness, chemical resistance, and adhesion to the substrate and components, but its opacity will also ensure that the circuit detail is visually obscured.

If you have any questions or would like more information about potting resins, their selection, handling, and applications, contact our Technical Support Team, and they will be more than happy to answer your queries. **DESIGN007**

Alistair Little is global business/technical director–resins–at Electrolube. To read past columns from Electrolube, click here. Also, visit www.I-007eBooks.com to download your free copy of Electrolube's book, *The Printed Circuit Assembler's Guide to... Conformal Coatings for Harsh Environments*, as well as other free educational titles.

Researchers Report Advances in Stretchable Rubbery Semiconductors, Integrated Electronics

Researchers from the University of Houston have reported significant advances in stretchable electronics, moving the field closer to commercialization.



Cunjiang Yu, Bill D. Cook Assistant Professor of mechanical engineering at the University of Houston and corresponding author on the paper, said the work could lead to important advances in smart devices such as robotic skins, implantable bioelectronics, and human-machine interfaces.

Carrier mobility—the speed at which electrons can move through a material—is critical for an electronic device to work successfully because it governs the ability of the semiconductor transistors to amplify the current.

Researchers discovered that adding minute amounts of metallic carbon nanotubes to the rubbery semiconductor of P3HT—polydimethylsiloxane composite—lead to improved carrier mobility by providing what Yu described as a "highway" to speed up the carrier transport across the semiconductor.

(Source: University of Houston)

Fast and Accurate Transmission Line Modeling

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

The ability to simulate complex PCB design has become a critical factor in the success of a project. Today's high-speed processors and SERDES interfaces coupled with sometimes unrealistic time-to-market requirements are pushing design teams toward more nimble development processes. However, there is no point in completing a design on time if it does not work!

To ensure the prototype has first-pass success, designers need to perform accurate board-level simulation, throughout the entire design process. But the challenge is how do you quickly perform the simulation if all the models for the board are not available and if the simulation setup time is prohibitive? Enter the I/O Buffer Information Specification (IBIS). This specification is a fast and accurate behavioral method of modeling input/output buffers based on I-V curve data derived from measurements or full circuit simulation.

Figure 1 depicts the Ibis (bird). With its greedy, little black eyes and its long, trash-probing beak, the Ibis has readily adapted to its environment. We Australians colloquially call it "the bin chicken" since its six-inch curved beak has been sculptured by evolution to effortlessly reach to the bottom of a Macca's (MacDonald's) fries container.

Getting back to simulation, before the release of the IBIS specification, SPICE transistor-level models were the only consistent method by which circuit models could be created. However, transistor-level models are not well suited to simulate an entire multilayer PCB containing several hundred nets and drivers. Also, semiconductor vendors that generate the models for their integrated circuits do not readily give these models out since they can disclose proprietary information that is confidential, including circuit nodal connections and underlying fabrication processes parameters. Meanwhile, the IBIS model does not require propri-

Figure 1: The Ibis. (Source: Australian Geographic)

etary information about the modeled circuit since no process or circuit design information is disclosed.

The IBIS models are accurate since nonlinear aspects of I/O structures as well as package parasitics, on-die termination (ODT), and ESD structures are considered in the model parameters. More recently, power-aware models have been specified to combine signal integrity (SI) and power integrity (PI) simulation. Since the IBIS is behavioral, the simulation time for a model can run some 25 times faster than a structural model such as that used in SPICE. In addition, IBIS does not have non-convergence issues encountered in SPICE models that prevent the simulator from reaching a valid solution within a certain number of iterations. Now, most EDA vendors support the IBIS specification as the defacto simulation standard.

IBIS models for many devices are available as free downloads from IC vendor support pages. IBIS provides the following:

- Faster simulation speed
- A large variety of I/Os in a single IBIS file so that easy system model simulation is possible
- The inclusion of signal integrity specifications, such as input logic thresholds, overshoots, etc.
- Power-aware properties introduced to provide simultaneous SI/PI analysis
- Elimination of non-convergence
- Strong support from virtually all EDA vendors
- Backward compatibility with models created under previous IBIS standards

At its core, a CMOS IBIS model (Figure 2) uses only a few tables of data to represent the behavioral characteristics of a buffer. Two sets of I-V tables represent the I_{DS} versus V characteristics of the pull-down and pull-up transistors, showing the dynamic impedance of the buffer. The switching behavior of the buffer is revealed through a set of V-T tables that capture the rising and falling edge transitions of the buffer driving resistive test loads. The capacitance of the buffer and the package RLC are also quantified. This information, plus the transmission line characteristics, provides an accurate model for SI simulation, but it lacks behavioral characteristics necessary for PI simulation. One of the major upgrades in the IBIS version 5.0 specification was the introduction of additional data tables to model buffer power characteristics (not shown). Models containing these data are known as power-aware IBIS models.

Let's look at a practical example of how to implement a transmission line simulation

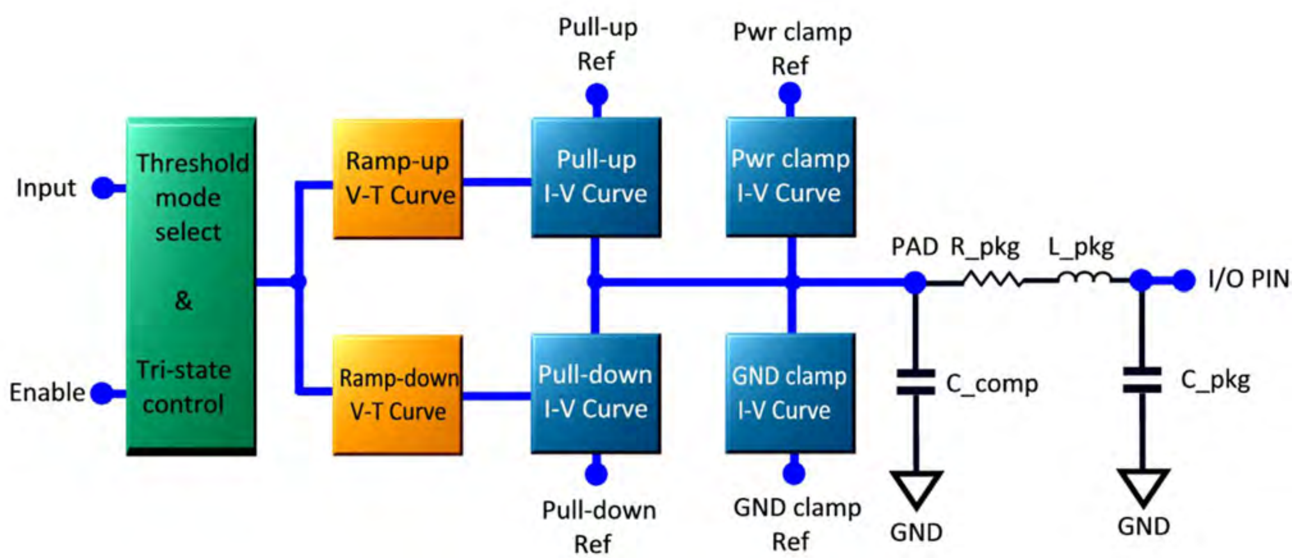


Figure 2: Building blocks of a CMOS buffer IBIS model.

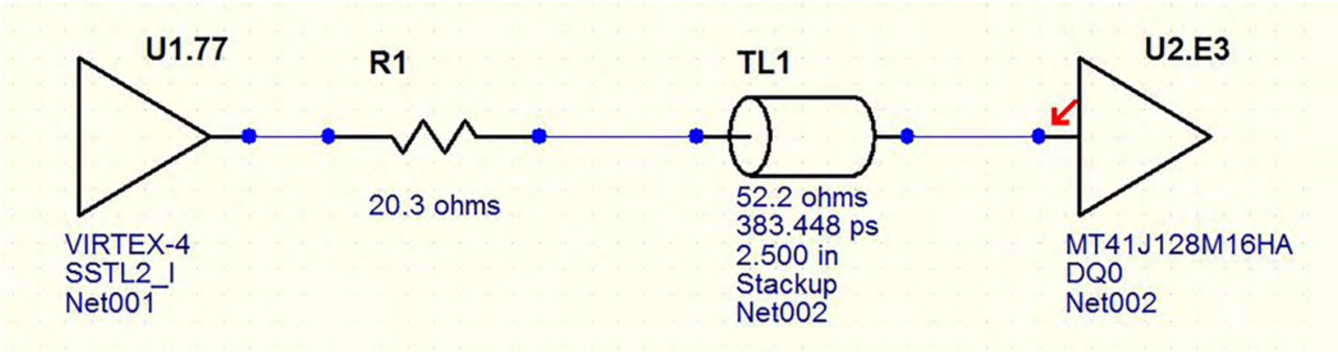


Figure 3: DDR2 data signal with a series terminator. (Source: HyperLynx)

using the IBIS model. I/O buffer and drive strength selection can be analyzed in pre-layout simulation. A vendor-provided IBIS model should contain all available drivers for each model, and may, for example, include buffer models with 8 mA, 12 mA, and 16 mA drive current. The mid-level 12-mA driver is generally required unless there is a long transmission line with multiple loads. This may be the case on a motherboard when driving a number of DIMM modules, for instance.

The schematic description that includes the stackup definition, arrangement of a network, its nodes, sequence, connecting transmission lines and vias is generically referred to as the interconnect topology. To avoid signal quality and timing issues and minimize manufacturing costs, thorough topology analysis is critical to the successful implementation of a high-speed interconnect. Ideally, this analysis should be done up-front before placement and routing.

Topology optimization involves:

- Selecting an optimal topology style for signal integrity, timing, and EMC
- Shortening traces and stubs to their critical length or shorter where possible

The most basic topology is a simple point-to-point interconnection between a driver and a receiver (Figure 3). This topology is commonly used for busses or otherwise grouped traces. A good example of this would be the data banks of DDRx memory. Left unterminated, these traces may be too long (more than 1/10 rise time), and reflections become problematic. Figure 3 also illustrates a Xilinx, Virtex 4 transceiver driving a DDR2 data signal into a long, 52.2-ohm transmission line. Initially, the signal was simulated with no series termination, resulting in the red waveform in Figure 4. The green waveform represents the terminated transmission line.

The impedance of the trace is extremely important, as any mismatch along the transmission path will result in a reduction in signal

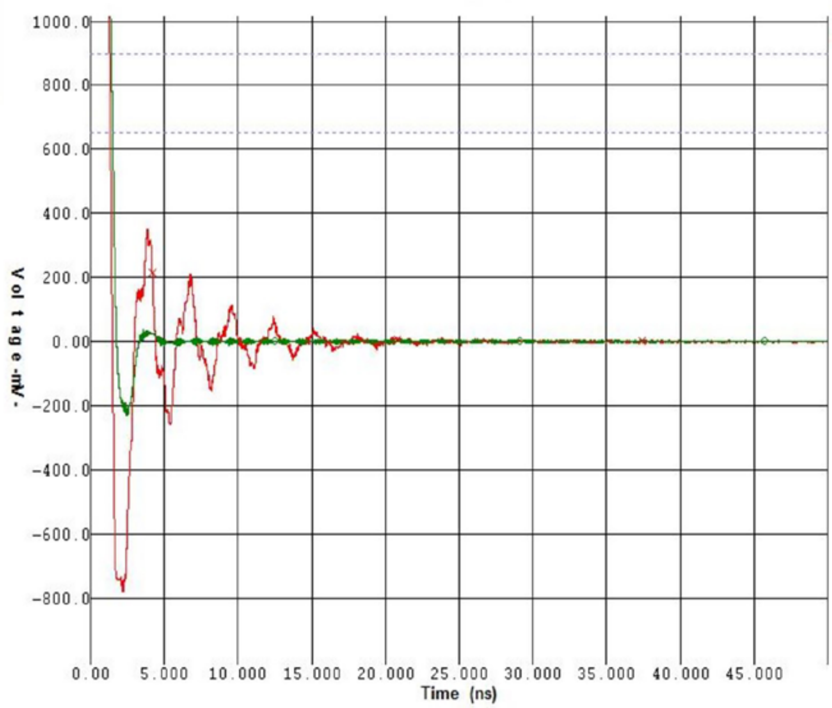


Figure 4: Ringing of the data signal due to reflections. (Source: HyperLynx)

quality and possibly the radiation of noise. Mismatched impedance causes signals to reflect back and forth along the transmission line, which results in ringing at the load (Figure 4). The ringing reduces the dynamic range of the receiver, eats into the noise budget, and can cause false triggering due to non-monotonic edges.

Reflections occur whenever the impedance of the transmission line changes along its length. This can be caused by unmatched drivers/loads, layer transitions, different dielectric materials, stubs, vias, connectors, and IC packages. By understanding the causes of these reflections and eliminating the source of the mismatch, a design can be engineered with reliable performance. For the perfect transfer of energy and to eliminate reflections, the impedance of the source must equal the impedance of the transmission line.

It is one thing to perfectly match the impedance and delay of the transmission lines, but using mainstream PCB layout software, unfortunately, one really has no idea what the driver impedance is, let alone the capability to match the driver to the impedance of the transmission line. The iCD Termination Planner addresses this issue (Figure 5).

First, the attributes required to determine the source impedance of the driver are extracted from an IBIS model I-V curves. Then, the required series termination resistance is calculated based on a distributed system to match the transmission line impedance for the selected stackup layer. The number of loads on the transmission line also has an impact on the required value of series termination, as the IC input inductance and capacitance tend to roll off the signal rise time. This can be adjusted from 1–6 loads and automatically compensated for in the calculation. If you do not have access to a board-level simulator, then this is a good option to easily avert ringing.

Modeling complex PCB designs does not have to be time-consuming and difficult. The topology can generally be automatically extracted from the PCB layout into a free-form schematic, providing all the transmission line, via, and stackup information required. The designer only needs to select the IBIS driver and load models plus a stimulus in the form of a set frequency or a pseudorandom bit stream (PRBS) to simulate

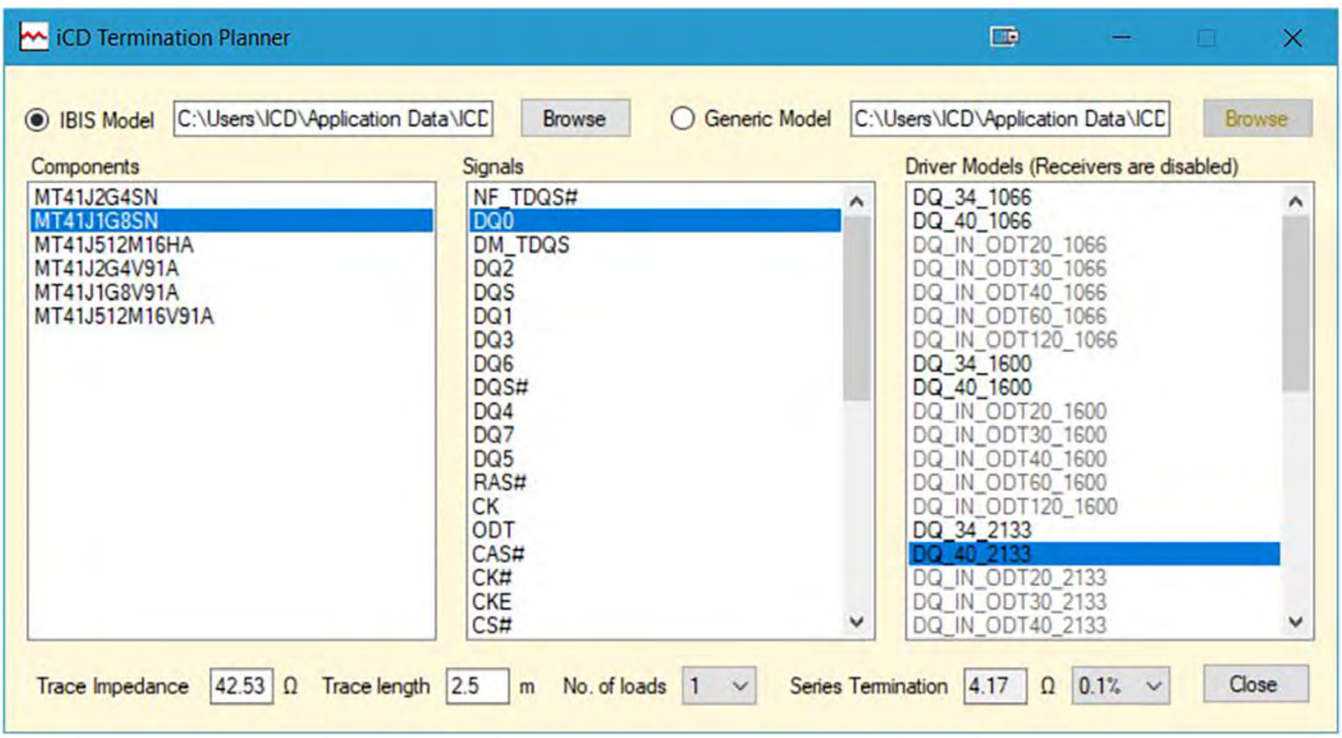


Figure 5: Matching a DDR3 driver IC to the transmission line. (Source: iCD Termination Planner)

the entire interconnect. The IBIS specification is a fast and accurate behavioral method of modeling high-speed transmission lines throughout the entire design process.

Key Points

- To ensure the prototype has first-pass success, designers need to perform intensive and accurate board-level simulation
- The IBIS specification is a fast and accurate behavioral method of modeling input/output buffers based on I-V curve data derived from measurements or full circuit simulation
- SPICE models are not well suited to simulating an entire multilayer PCB containing several hundred nets and drivers
- SPICE models can disclose substantial information that is confidential, including circuit nodal connections and underlying fabrication processes parameters
- The IBIS model does not require proprietary information about the modeled circuit since no process or circuit design information is disclosed
- Since the IBIS is behavioral, the simulation time for a model can run some 25 times faster than a structural model, such as that used in SPICE
- A CMOS IBIS model uses only a few tables of data to represent the behavioral characteristics of a buffer
- One of the major upgrades in the IBIS version 5.0 specification was the introduction of power-aware models
- The interconnect topology includes the stackup definition, arrangement of a network, its nodes, sequence, and connecting transmission lines and vias
- The impedance of the trace is extremely important, as any mismatch along the transmission path will result in a ringing, reduced signal quality, and possibly the radiation of noise
- Using mainstream PCB layout software, one really has no idea what the driver impedance is, let alone the capability to match the driver to the impedance of the transmission line **DESIGN007**

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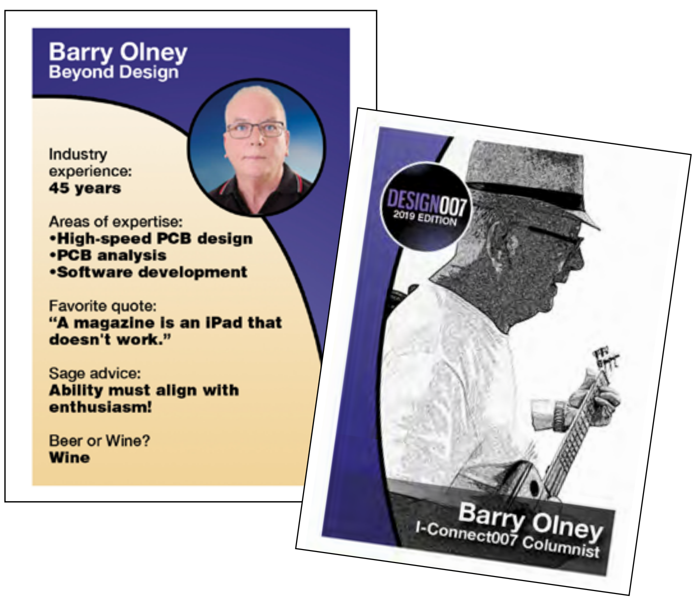
Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded from www.icd.com.au. To read past columns or contact Olney, click here.



How Copper Properties Impact PCB RF and High-speed Digital Performance

Lightning Speed Laminates

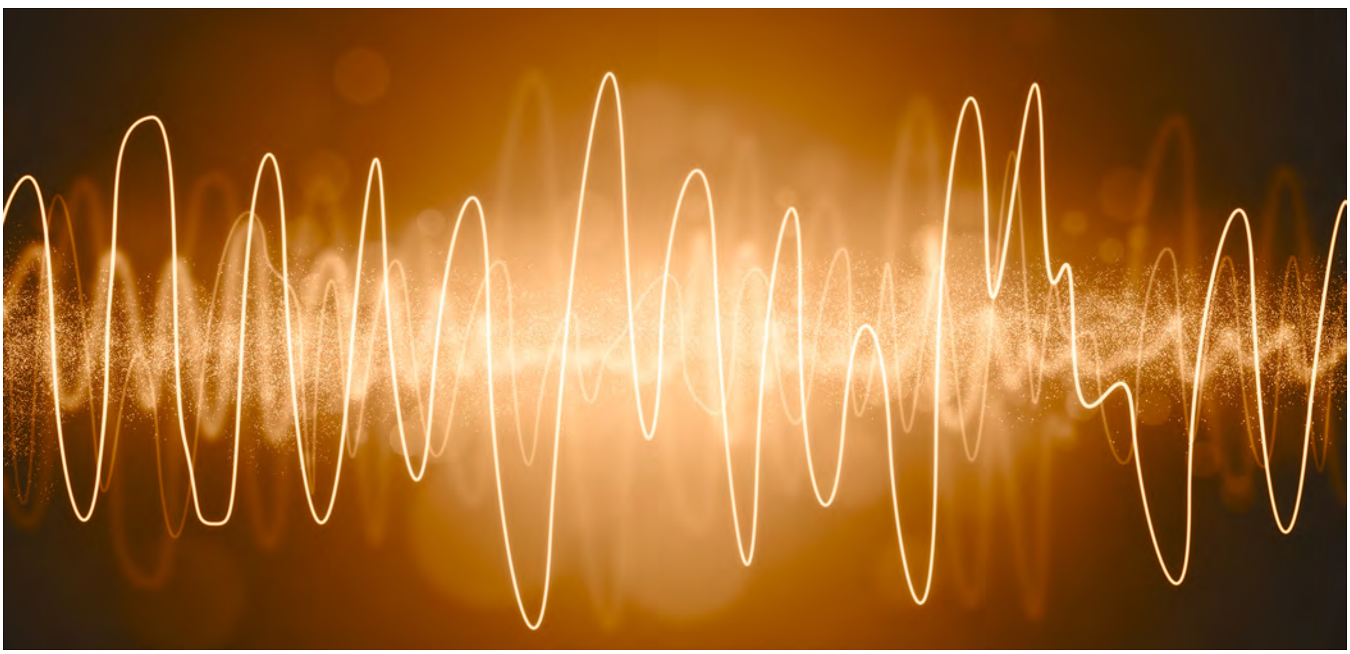
by John Coonrod, ROGERS CORPORATION

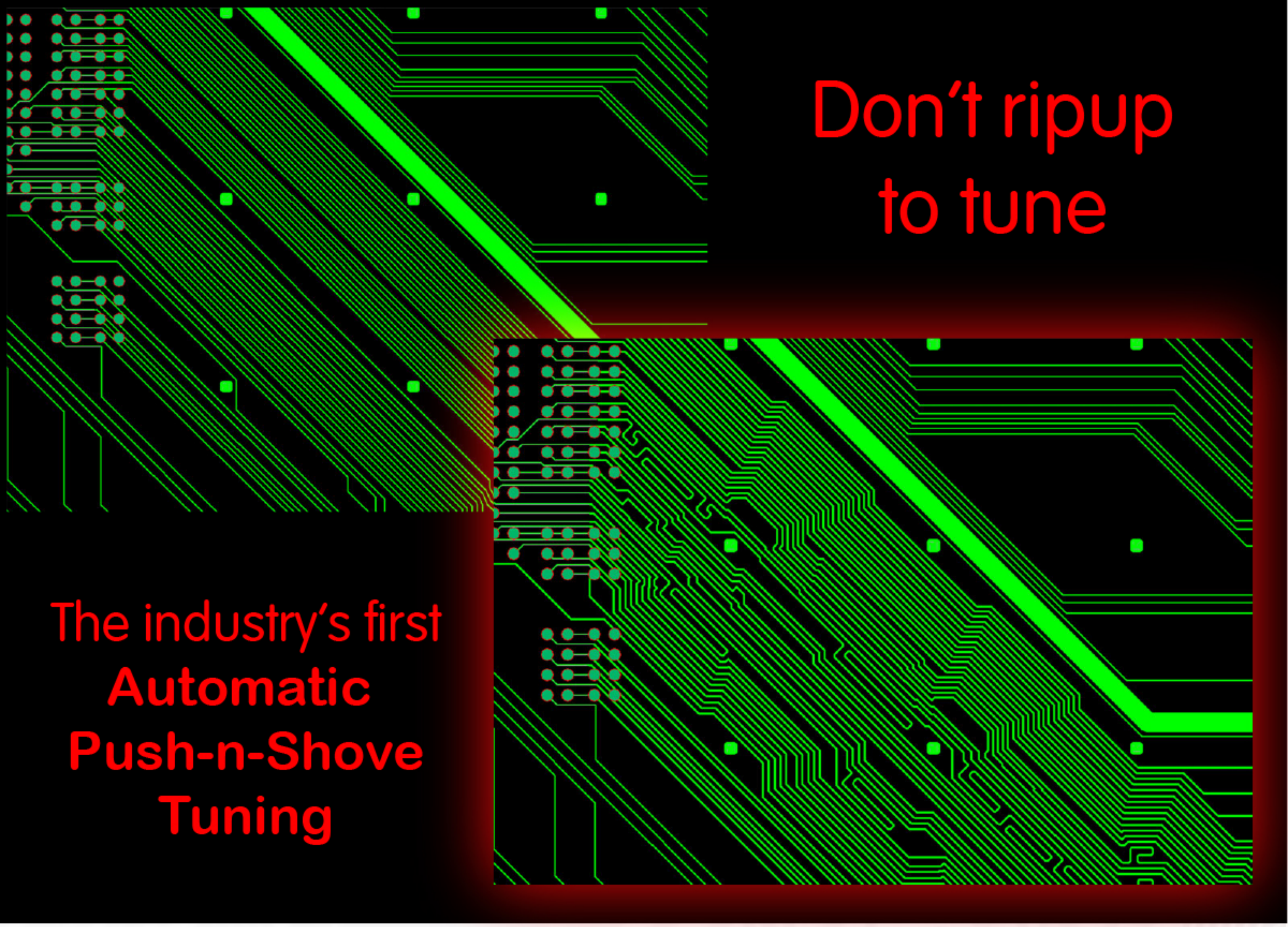
It has been well known in the RF industry for many years that copper surface roughness impacts RF performance of PCBs. This analogous statement also applies to high-speed digital applications. To explain the copper surface roughness issue, take a simple two-layer copper circuit, for example.

The circuit is a microstrip with a signal conductor on the top copper plane and a ground plane on the bottom of the circuit. Additionally, the concept of skin depth and wave propagation should be considered. Skin depth is the depth within the cross-sectional area of the copper where the majority of the RF current resides and is dependent on frequency. At lower frequencies, the RF current will have a thicker skin depth and use more of the conductor. At higher frequencies, the skin depth is thinner, and less of the conductor is used by the RF current. For wave propagation, the electromagnetic wave that propagates on the microstrip circuit will be slower for a circuit using a higher dielectric constant (Dk) material. Using a lower-Dk material, the wave propagation is faster, and the propagation delay is reduced.

Rogers has studied copper surface roughness extensively and has a lot of information to share for the interested reader. We know if a comparison is done on two identical circuits with one using a high-Dk material and the other a low-Dk material, the circuits will have slower and faster wave propagation, respectively. However, we found other circuit properties can alter the wave propagation speed, and one of them is the copper surface roughness. To be specific, the copper surface roughness is the roughness at the substrate-copper interface.

Further, we have done experiments where the same material was used with the same mi-

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crostrip design, and the only difference was the copper type. In these experiments, we consistently saw that circuits with a rougher copper surface had a slower wave propagation compared to circuits with a smoother surface. A rougher copper will slow the wave, and a slower wave is perceived by the circuit as a higher Dk, even though the Dk of the material is the same for both circuits. When extracting the Dk value from circuit performance, the circuit with the rougher copper will have a higher Dk value than the circuit with a smoother copper. Also, we found that wave propagation is more affected by the copper surface roughness in circuits made using a thinner substrate versus circuits made with a thicker substrate.

When extracting the Dk value from circuit performance, the circuit with the rougher copper will have a higher Dk value than the circuit with a smoother copper.

The effect that copper surface roughness has on wave propagation is also frequency dependent, and at low frequencies, the copper surface roughness may have little or no impact on the wave velocity. Frequency dependency is due to skin depth and at low frequencies where the skin depth is thick. The roughness is a small percentage of the cross-sectional area of the conductor being used by the RF current; the effect of the copper roughness has little influence on the wave propagation. However, at higher frequencies—specifically, frequencies where the skin depth is equal to or less than the copper surface roughness—the roughness will have a significant impact on the wave propagation properties of the circuit.

For an RF PCB using copper with a rougher surface, the copper surface will cause an increase in conductor loss, slower wave velocity, and a higher effective Dk. For a high-speed digital PCB using copper with a rougher surface, the copper will cause an increase in insertion loss and propagation delay, and a decrease of the eye opening in an eye-diagram, typically. Many years ago—when digital rates were slower, and the Nyquist frequency was lower—the influence copper surface roughness had on these circuits was minimal. Now, with faster digital rates and higher Nyquist frequencies, the potential effects that copper surface roughness has on these circuits can be substantial.

With many new applications using millimeter-wave technology, which is RF at very high frequencies, the copper surface roughness can have a very large impact on RF performance for these circuits. Insertion loss and phase response of millimeter-wave circuits can be greatly impacted by copper surface roughness. All copper types used in the PCB industry have normal surface variation. The natural trend is that a copper with a rough surface will have much more roughness variation than copper with a smooth surface. The copper surface roughness variation can cause phase variation from circuit to circuit.

Even though my example uses a two-layer copper circuit, a common concern in building multilayer PCBs is that the copper surface roughness may have more impact on the circuit electrical performance than the designer would anticipate. The PCB fabricator will often have a choice of what type of copper to use on certain layers within the multilayer PCB. Typically, their decision is based on their desire to build a robust circuit. To optimize the electrical performance of a circuit, copper surface roughness also needs to be considered.

For more details on this subject, please contact your PCB materials provider. DESIGN007

John Coonrod is technical marketing manager at Rogers Corporation. To read past columns or contact Coonrod, click here.

MilAero007 Highlights

BAE Systems Updates F-35 Electronic Warfare Systems ▶

BAE Systems has upgraded its EW systems for the global fleet of fifth-generation F-35 Lightning II fighter aircraft.

Benchmark Electronics Appoints Jeff Benck as President and CEO ▶

Benchmark Electronics Inc.'s board of directors has appointed Jeff Benck as president and CEO.

ANU Research Set to Shake-up Space Missions ▶

A new study from the Australian National University (ANU) has found a number of 2D materials that can not only withstand being sent into space but could potentially thrive in the harsh conditions.

Video: Five-year Standard Committee Collaboration on JS-001 ▶

David Hillman from Collins Aerospace and IPC's Teresa Rowe speak with Editor Dan Feinberg about how a seemingly simple question resulted in years of committee work to develop the JS-001 standard on the use of conformal coatings and avoiding tin whiskers.

High-powered Fuel Cell Boosts Electric-powered Submersibles, Drones ▶

A team of engineers in the McKelvey School of Engineering at Washington University in St. Louis has developed a high-power fuel cell that could power a variety of transportation modes—including unmanned underwater vehicles, drones and eventually electric aircraft—at a significantly lower cost.

NASA Looks to the Future, Seeks Next Level Visionary Aerospace Concepts ▶

NASA is looking for trailblazing ideas that could one day change what's possible in space. The NASA Innovative Advanced Concepts (NIAC) program is seeking Phase II proposals for the continuation of Phase I research studies.

Zentech Hosts UMBC Advanced Manufacturing Graduates ▶

Zentech Manufacturing recently hosted twenty-four graduating seniors from the University of Maryland Baltimore Campus (UMBC) at its Baltimore headquarters location.

Collins Elbit Vision Systems Marks F-35 Helmet Mounted Display System Delivery Milestone ▶

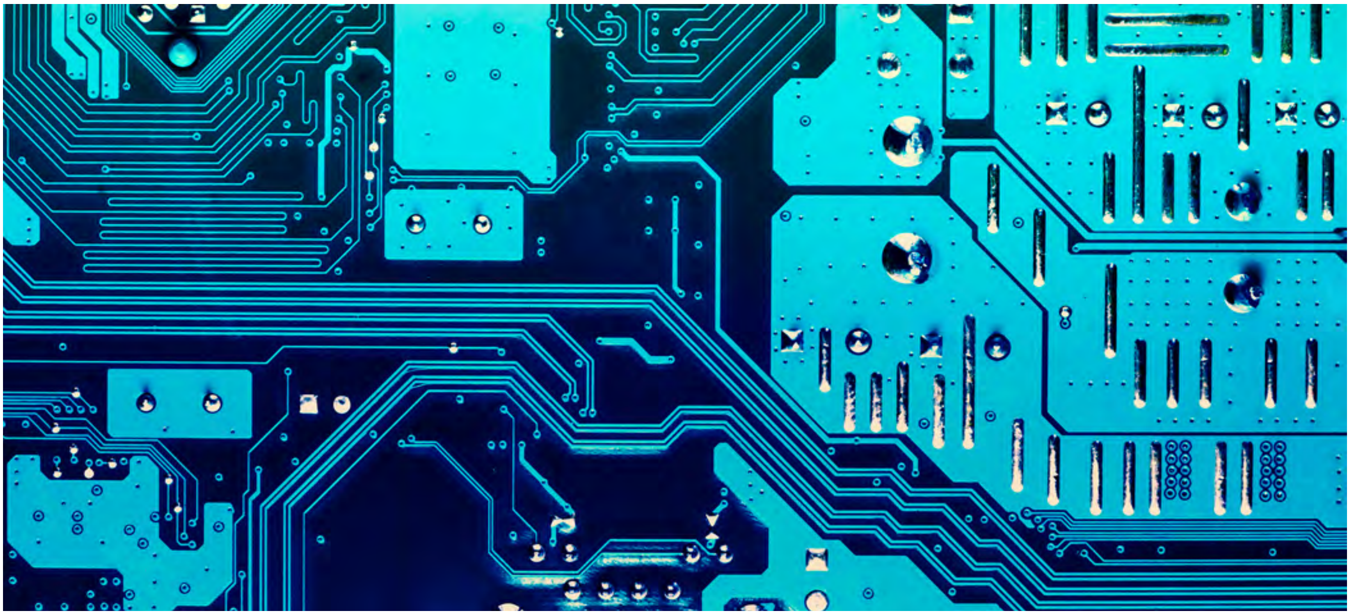
Collins Elbit Vision Systems (CEVS) recently celebrated the 1,000th delivery milestone of the F-35 Helmet Mounted Display (HMD)System.

2020 Army Budget Begins 'Dramatic Shift' ▶

An Army budget drill that identified $30 billion in savings was partly about finding money for future modernization, according to Undersecretary of the Army Ryan D. McCarthy during a breakfast hosted by the Association of the U.S. Army's Institute of Land Warfare.

Cicor Strengthens Testing Capabilities at Radeberg Facility ▶

In January 2019, the Cicor site in Radeberg acquired a new pull and shear tester for mechanical testing of the strength of electronic packaging superstructures.



EM Modeling: The Impact of Copper Ground Pour on Loss and Impedance

Article by Chang Fei Yee
KEYSIGHT TECHNOLOGIES

This article briefly introduces the general purposes of copper ground pour on printed circuit boards. Subsequently, the impact of copper ground pour on PCB channel loss in terms of insertion loss and impedance in terms of time domain reflectometry (TDR) is studied with electromagnetic modeling using Mentor HyperLynx.

Introduction

Copper ground pours are created by filling open, unpopulated, or unrouted areas on outer layers of the PCB with copper. Subsequently, copper fill is hooked up to ground planes on inner layers with stitching vias as depicted in Figure 1. Copper ground pours on outer layers provide extra shielding against electromagnetic radiation by signals on inner layers. Besides that, copper pour also serves as a heat sink for the voltage regulator module on PCBs. In terms of manufacturability, copper pour reduces the possibility of PCB warpage during reflow by balancing the amount of copper on each side of the PCB.

However, copper ground pour comes with some disadvantages, as there is a change in

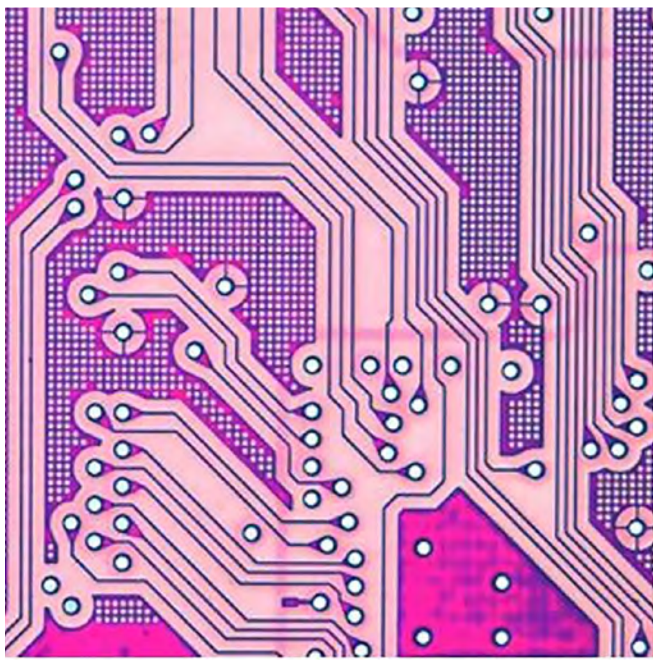


Figure 1: Top view of the PCB with copper ground pours.

impedance of PCB trace adjacent to ground pour (i.e., impedance decreases when copper pour becomes closer to the PCB trace). As a result, the impedance mismatch contributes additional PCB loss to the transmission line at a high-frequency range.

Analysis and Results

To study the impact of copper pour on PCB channel loss in terms of insertion loss and impedance in terms of TDR, five models of 1″ single-ended microstrip listed in Table 1 were created. The simulation topology is shown in Figure 2. For model 1A, a microstrip trace 5 mils wide and 1 oz. thick is laid out 2.65 mils above the reference plane insulated by low-loss dielectric substrate material. This trace is sandwiched between two ground traces on the same outer layer. The spacing between each adjacent ground trace and the signal trace is 1x the signal trace width. Meanwhile, the spacing between each ground and signal trace is set as 2x, 4x, 6x, and 8x for model 1B, 1C, 1D and 1E, respectively.

Model	Description
1A	Spacing between adjacent ground and signal trace, each side: 1x trace width (5 mils)
1B	Spacing between adjacent ground and signal trace, each side: 2x trace width (10 mils)
1C	Spacing between adjacent ground and signal trace, each side: 4x trace width (20 mils)
1D	Spacing between adjacent ground and signal trace, each side: 6x trace width (30 mils)
1E	Spacing between adjacent ground and signal trace, each side: 8x trace width (40 mils)

Table 1: List of models for copper pour effect on PCB single-ended microstrip.

The TDR plots depicted in Figure 3a indicates that microstrip experiences an impedance mismatch of 1 ohms when its distance from the adjacent ground at each side is set as 1x the trace width (model 1A). The impedance mismatch is getting smaller or closer to the nominal 50 ohms when the ground at each side is further away from the signal trace or beyond 2x the trace width.

However, with reference to insertion loss plots depicted in Figure 3b, model 1A with adjacent ground-signal spacing of 1x the trace width encounters 1.5-dB channel loss at 10 GHz. When adjacent ground-signal spacing is increased to 2x the trace width, the channel loss is reduced by 0.75 dB. Beyond adjacent

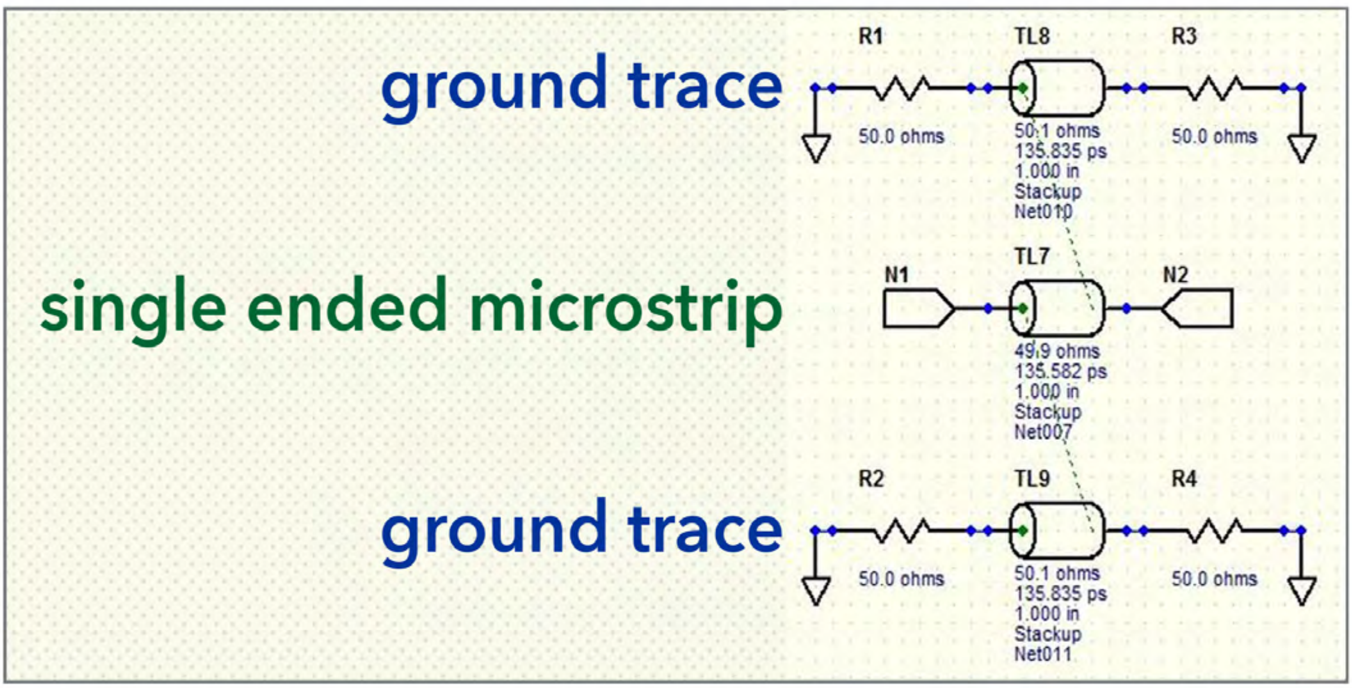


Figure 2: Single-ended microstrip model in Hyperlynx.

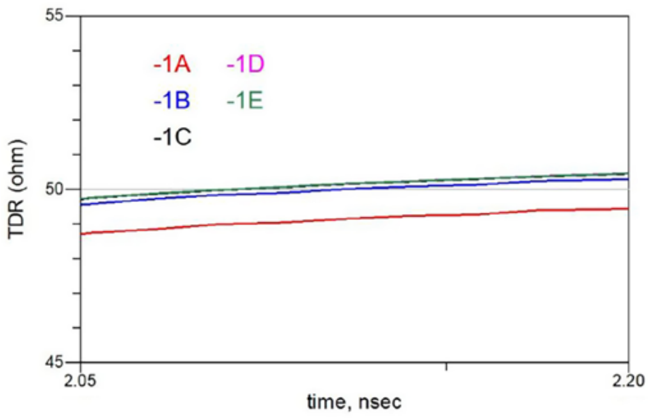


Figure 3a: TDR plots for models listed in Table 1.

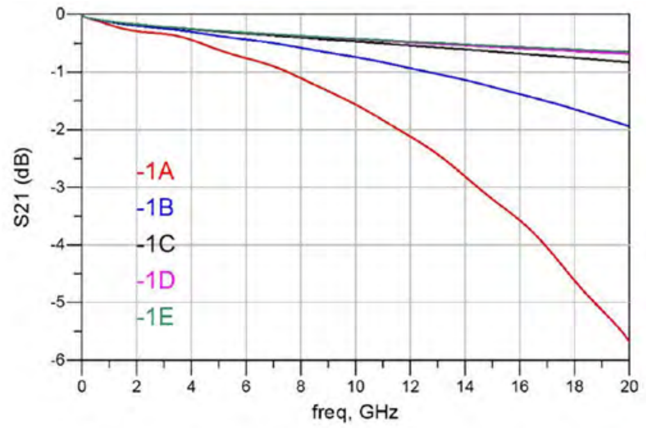


Figure 3b: Insertion loss plots for models listed in Table 1.

ground-signal spacing of 4x the trace width, extra loss reduction of 0.25 dB is achieved.

The experiment is repeated on differential microstrip with five models of 1″ differential microstrip listed in Table 2. Simulation topology is depicted in Figure 4. For model 2A, microstrip traces (5-mil trace width, 7-mil intra-pair spacing, and 1 oz. in thickness) is laid out 3 mils above the reference plane insulated by low-loss dielectric substrate material.

This differential pair is sandwiched between two ground traces on the same outer layer. The spacing between each adjacent ground

Model	Description
2A	Spacing between adjacent ground and differential pair, each side: 1x trace width (5 mils)
2B	Spacing between adjacent ground and differential pair, each side: 2x trace width (10 mils)
2C	Spacing between adjacent ground and differential pair, each side: 4x trace width (20 mils)
2D	Spacing between adjacent ground and differential pair, each side: 6x trace width (30 mils)
2E	Spacing between adjacent ground and differential pair, each side: 8x trace width (40 mils)

Table 2: List of models showing the effect of copper pour on differential microstrip.

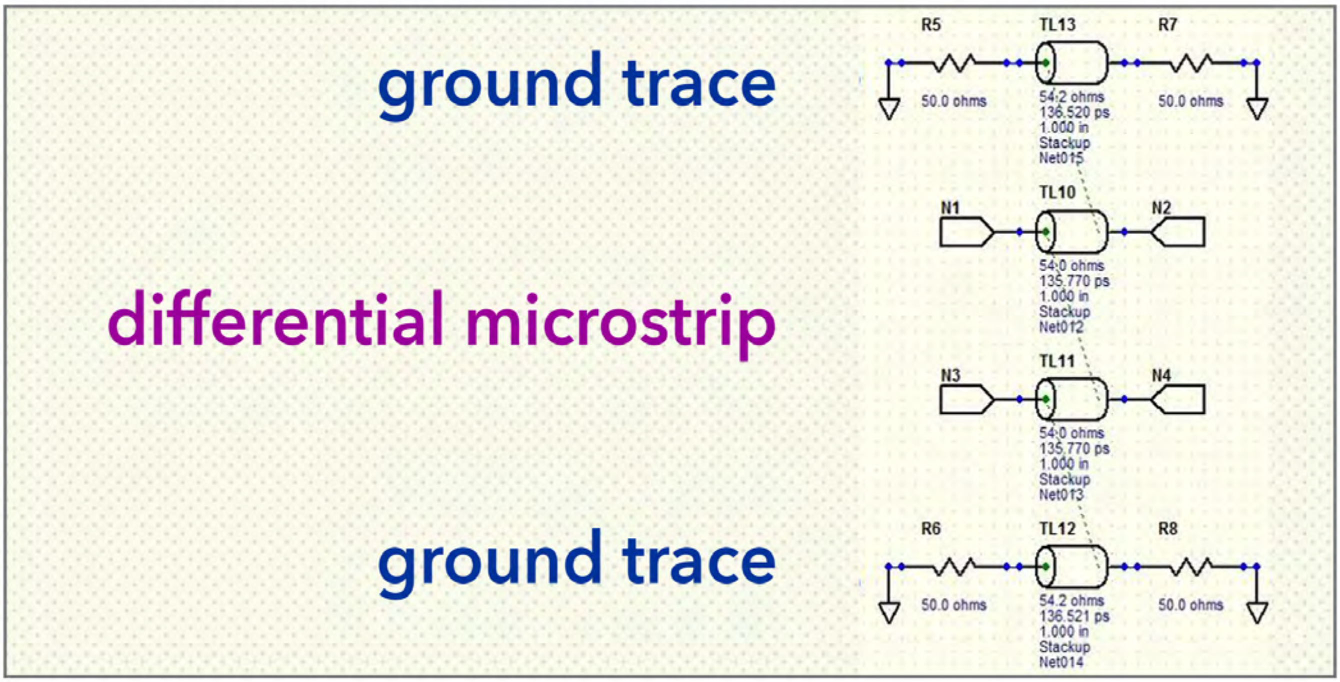


Figure 4. Differential microstrip model.

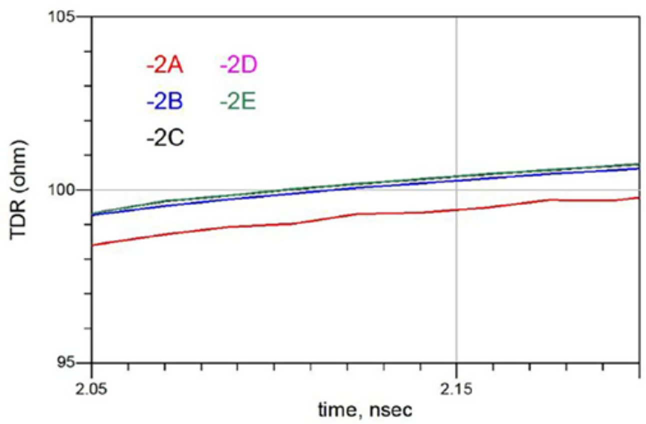


Figure 5a: TDR plots for models listed in Table 2.

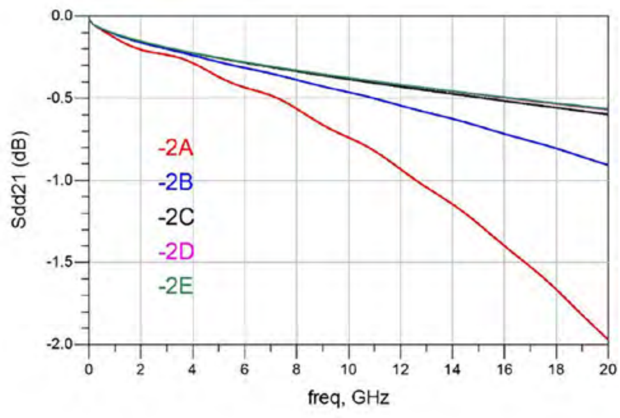


Figure 5b: Insertion loss plots for models listed in Table 2.

trace and the differential pair is 1x the signal trace width. Meanwhile, the spacing between each ground and signal trace is set as 2x, 4x, 6x, and 8x for model 2B, 2C, 2D, and 2E, respectively.

The TDR plots depicted in Figure 5a indicate that microstrip experiences an impedance mismatch of 1 ohms when its distance from the adjacent ground at each side is set as 1x the trace width (model 2A). The impedance mismatch is getting smaller or closer to the nominal 100 ohms when the ground at each side is further away from the differential pair (i.e., beyond 2x the trace width).

However, with reference to insertion loss plots depicted in Figure 5b, model 2A with adjacent ground-signal spacing of 1x the trace width encounters 0.75-dB channel loss at 10 GHz. When adjacent ground-signal spacing is increased to 2x the trace width, the channel loss is reduced by 0.3 dB. Beyond adjacent ground-signal spacing of 4x the trace width, extra loss reduction of 0.1 dB is achieved.

Summary

For PCBs with signal routing beyond 1-GHz transmission, the copper ground pour must be set at least 4x the signal trace width away from the signal routing to minimize the impedance mismatch and channel loss. **DESIGN007**

References

1. Olney, B. "Ground Pours–To Pour or Not to Pour."
2. King Sun PCB Technology, "Some Pros and Cons About PCB Copper Pour," December 27, 2017.

Chang Fei Yee is a hardware engineer with Keysight Technologies. His responsibilities include embedded system hardware development, and signal and power integrity analysis.

New Graphene-based Device Paves the Way for Ultrasensitive Biosensors

Researchers from the University of Minnesota College of Science and Engineering have developed a unique new device using graphene that provides the first step toward ultrasensitive biosensors.

"To detect and treat many diseases, we need to detect protein molecules at very small amounts and understand their structure," said Sang-Hyun Oh, University of Minnesota electrical and computer engineering professor and lead researcher on the study.

University of Minnesota researchers combined graphene with nanosized metal ribbons of gold and utilized a homegrown high-tech nanofabrication technique called "template stripping" to create an ultra-flat base layer surface for the graphene. (Source: University of Minnesota)

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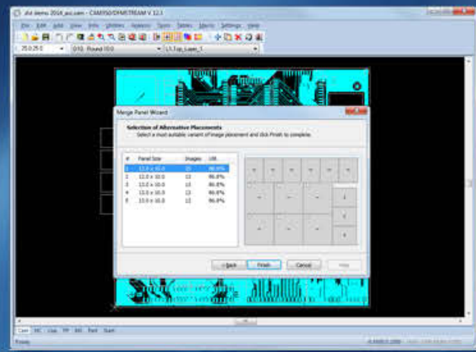

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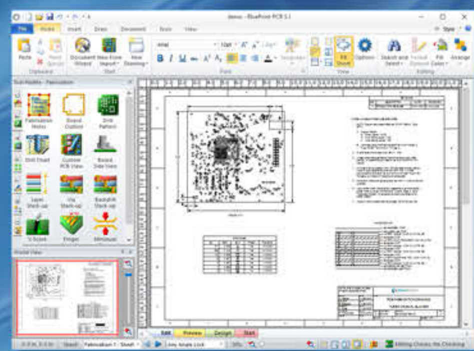

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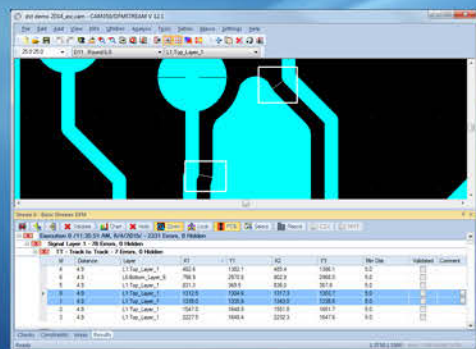

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Editor Picks from PCBDesign007

1 Todd Westerhoff Discusses His New Position and Much More ▶


Todd Westerhoff

At DesignCon, Andy Shaughnessy met with our old friend Todd Westerhoff. Todd recently joined Mentor, a Siemens Business, and discussed his new job responsibilities, his drive to get more designers and engineers to use SI tools, and the increasing value of cost-reduced design techniques versus overdesigning PCBs.

2 Beyond Design: Not All PCB Substrates Are Created Equal ▶

PCB substrates are all around us in every gadget we use. It is a carrier for the electronic devices and the signal and power interconnects and is usually planar in structure with conductors separated by insulating dielectric materials. However, each product has a specific performance requirement and may need a distinct type of substrate to comply with the product's specifications.

3 Embedding Components, Part 7—Semiconductor Placement and Termination Methodologies ▶

Progress in developing high-density embedded-component substrate capability has accelerated through the cooperation and joint development programs between many government and industry organizations and technical universities.

4 The Digital Layout: Cascade Designers Council Chapter and 2019 Activities ▶


Stephen Chavez

Our CID+ class had four people enrolled who came from around the area. All who attended learned about how board materials affected their designs, including EMI, EMC, impedance control, power distribution techniques, board stackups, and placement strategies in more detail than what was in the CID.

5 Linda Mazzitelli: PTC Goes all in on ECAD/MCAD Collaboration ▶


Linda Mazzitelli

At AltiumLive Munich, Andy Shaughnessy ran into Linda Mazzitelli of PTC. Linda has worn a lot of hats in the PCB design world—she's even married to a designer. Linda discussed her current work at PTC and the apparent convergence of ECAD and MCAD, which many think has been a long time coming for this industry.

6 Cherie Litson on ECAD/MCAD and Training the Next Generation ▶


Cherie Litson

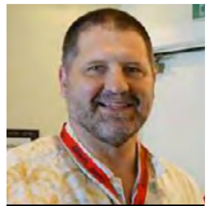
Cherie Litson, CID+, was one of the instructors at AltiumLive Munich. Andy Shaughnessy asked her to discuss some of the topics she covered in her class, and what the future of PCB design will look like. How are we going to pass down all of this design knowledge to the next generation?

7 EMA: Cadence Moves Simulation Further Up in the Design Cycle ▶


Chris Banton

Cadence Design Systems recently integrated more of its Sigrity capabilities into the front end of its PCB design tools. During DesignCon, Chris Banton of EMA Design Automation spoke with me about how this drive for "model-less analysis" benefits the PCB designer who can now access signal and power integrity, DFM, and electrical rule checking functionality early in the design process and have fewer issues later.

8 Carl Schattke on Stackup Design and Managing the Component Shortage ▶


Carl Schattke

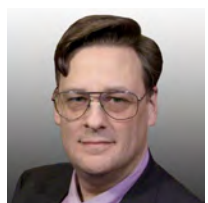
At AltiumLive, Carl Schattke, CID+, a lead PCB designer with an American automaker, and TTM's Julie Ellis taught a packed class on good stackup practices complete with plenty of slides showing examples of all kinds of stackups. After class, Carl explained why the stackup is often the root of manufacturing problems downstream, and why today's discrete component shortages are likely to be around for quite some time.

9 The Bare (Board) Truth: Eliminate Confusion ▶


Mark Thompson

This column will address eliminating confusion that creates remakes both from the end-user/designer and the fabrication house. Let's say you've asked for a material type on your drawing that is not either readily available or used by your fabricator.

10 Tim's Takeaways: A Job Worth Doing ▶


Tim Haag

I get it. We PCB designers are made of the kind of tough stuff where we will work ourselves to death if given the chance. But in our all of our efforts, are we really doing it right, or could we somehow be doing it better? Let's take a moment to consider some other ways that we might help ourselves to improve.

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- Possess the ability to calm difficult situations with customers, initiate a step-by-step plan, and involve other technical help quickly to find resolution.

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Maker Faire Bay Area ▸
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Medical Electronics Symposium 2019 ▸
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SMTA International ▸
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